xTCA for Physics

Jorge Sousa[1]

Member PICMG Physics Standards Committee

On behalf of IST/IPFN[1] and PICMG Physics HWG contributors

[1] Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico, Universidade Técnica de Lisboa, 1049-001 Lisboa, Portugal
http://www.ipfn.ist.utl.pt

xTCA for Physics Objectives

- ATCA and MicroTCA is the first platform available to the physics community providing:
  - all-serial communication platform;
  - both complex experiment controls and large, high bandwidth and throughput data acquisition systems;
  - a multi-layer highly scalable managed platform architecture;
  - the highest possible system performance, availability and interoperability.

- xTCA for Physics extensions goal:
  - Improve the management system that is an important tool for the instrumentation and control systems of complex scientific machines and instruments;
  - Extend the ATCA and MTCA telecom standards hardware for physics controls and applications;
  - Provide Software Guidelines to promote interoperability of modules designed by industry and laboratories, in particular focusing on middleware and generic application interfaces such as Standard Process Model, Standard Device Model and Standard Hardware API.

New Features Required for Physics Hardware

- To achieve high availability in a complex physics system requires three main features common to ATCA/µTCA:
  1. Modular architecture
  2. N+1 or N+M redundancy of single-point-of-failure modules (whose malfunction could stop operation of the machine or experiment)
  3. Intelligent platform management for quick isolation of faults and hot-swap
- In addition, physics modules need a few extended features not covered by current specifications:
  4. Rear transition modules (RTM) with standardized interconnects and management features
  5. Extended real estate on cards for high performance analog conversion, signal conditioning and calibration circuitry
  6. Extended options for backplane distribution of high precision timing, triggering and machine synchronization of modules and groups of modules
- The goal of xTCA is to accomplish the latter features with backward compatibility to existing designs of processors, modules or carrier cards that use the standard backplane.

xTCA Extensions

The following slides will present:

A. ATCA RTM Interface Extensions (PICMG 3.8)

B. Timing Extensions for ATCA (PDG.0)

C. MicroTCA µRTM Extensions (MTCA.4)

D. Timing Extensions for AMC/µTCA

E. Software Guidelines Development

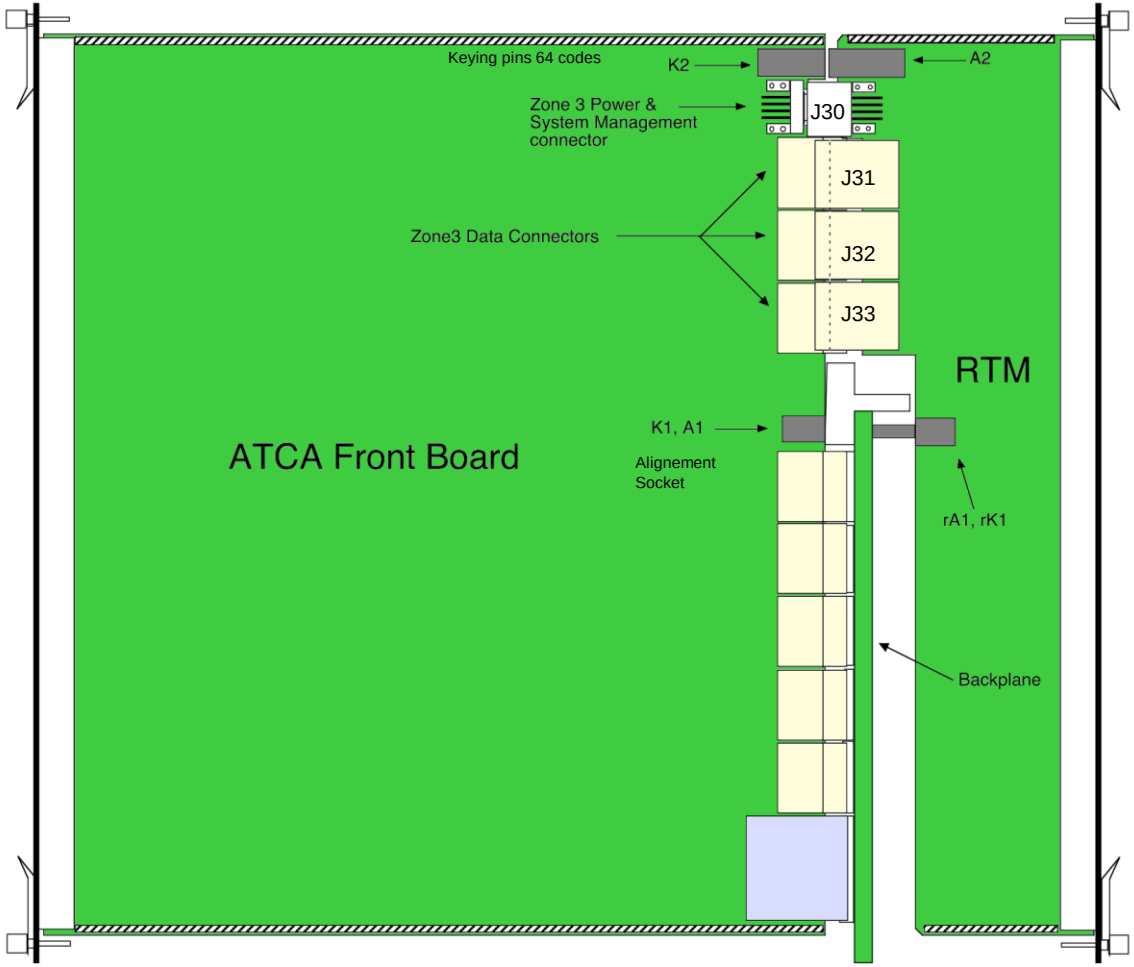
A. xTCA RTM Interface (PICMG 3.8)

A. ATCA RTM Interface (PICMG 3.8)

- PICMG 3.0 specified the mechanics for the RTM but no Zone 3 connectors

- A Physics RTM interface (PICMG 3.8), now defines of the following elements:
  - Up to 3 ADF connectors (each has 4-row by 10 column of differential pairs) for I/O.
  - A power and management connector – RTM appears to the system as if it were an AMC module.
  - The interface description and mechanical keying solution.
  - New RTM mechanical layout.
  - The standard management interface additions.

Front and Read Board Assembly



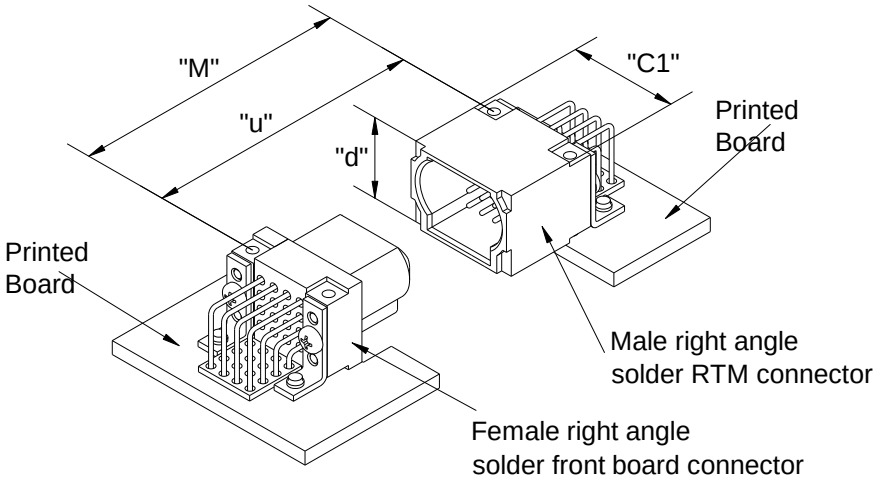
A. Alignment/Keying

- ATCA spec defines mechanical alignment and “keying” methods
- Mechanical keying codes tell about the electrical interface
  - Mating is prevented if modules are not electrically compatible and damage could occur – mainly an analog signal issue.

B. Power & System Management

C. User I/O – ADF Connectors

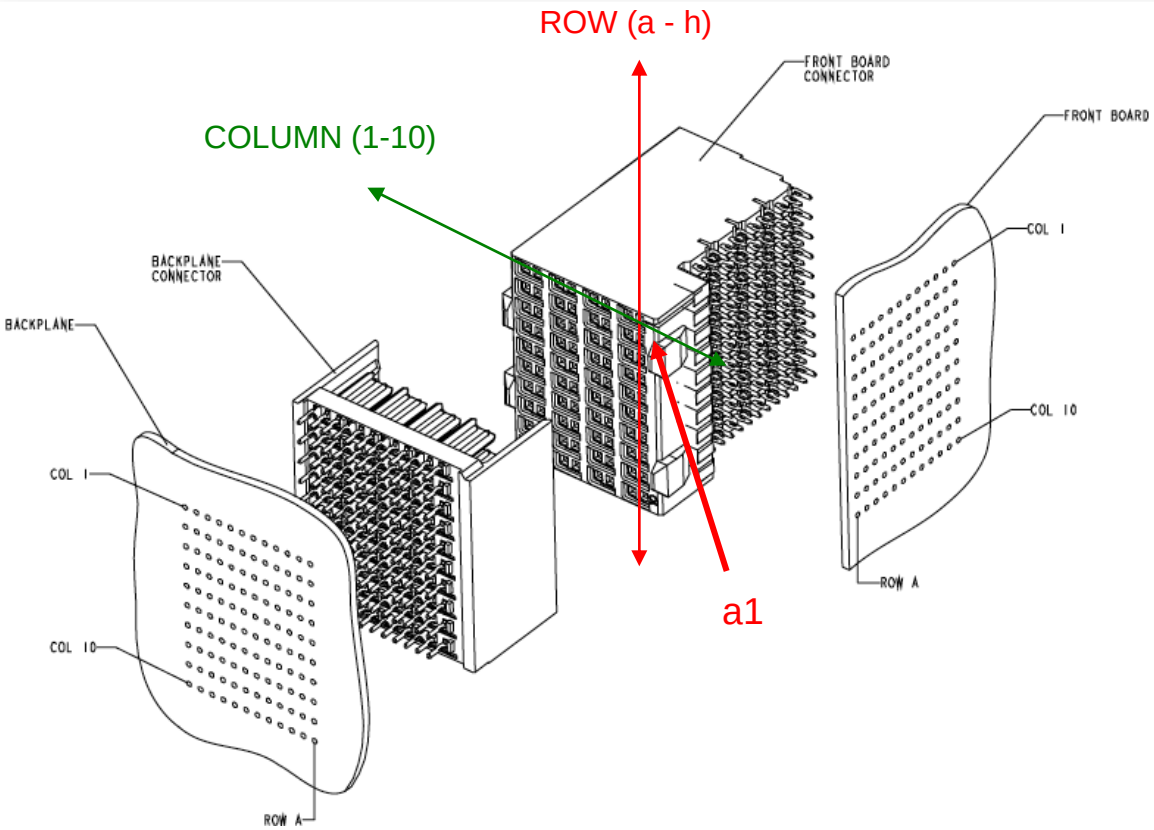
B. Power and System Management connector (J30)



- Connector defined in Zone 3 to perform similar function as Zone 1 connector.
- Positronic Industries modified an existing connector that met the requirements.
  - MP (+3.3V, 500 mA) 2 pins
  - PWR (+12V, 5 A) 4 pins
  - ENABLE# 1 pin
  - PS# 1 pin
  - SCL/SDA (I^2C) 2 pins
  - JTAG 4 pins
  - Reserved (power +?) 2 pins

- System management system checks the e-key to determine if modules are compatible and can be fully powered on.
- The optional Enable# and PS# signals in the IRTM.0 specification are mandatory.
- The PS# is a last mate pin for hot swap.
- Identification codes are assigned to each RTM.

C. RTM User I/O – ADF connectors



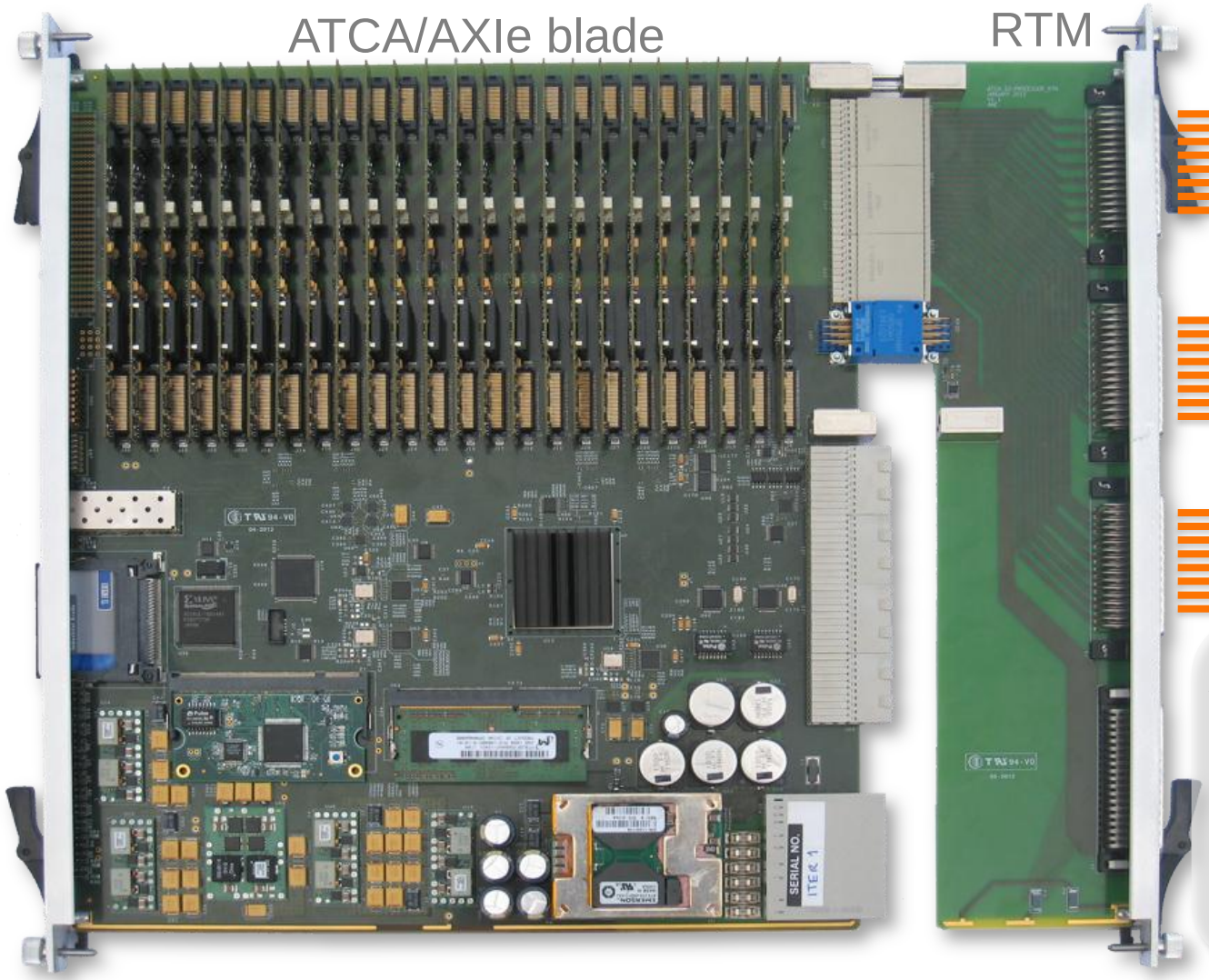
- Only generic ports (diff pair) are defined.
- Channel grouping defined by the applications.

- The Physics RTM uses the same connectors as in Zone 2 of the ATCA specification.
- There are up to 120 differential pairs or 240 single ended signals that can be connected between the ATCA module and its RTM.
- Each pair has an associated ground pin.
- Allow flexible use of ports: Transmit only, Receive only, T/R, or two single ended TR,TT or RR.

RTM User I/O – Pin assignement

Pairs → Row# ↓	Gnd	H	G	Gnd	F	E	Gnd	D	C	Gnd	B	A
1	GND[9]	P3[9]-	P3[9]+	GND[9]	P2[9]-	P2[9]+	GND[9]	P1[9]-	P1[9]+	GND[9]	P0[9]-	P0[9]+
2	GND[8]	P3[8]-	P3[8]+	GND[8]	P2[8]-	P2[8]+	GND[8]	P1[8]-	P1[8]+	GND[8]	P0[8]-	P0[8]+
3	GND[7]	P3[7]-	P3[7]+	GND[7]	P2[7]-	P2[7]+	GND[7]	P1[7]-	P1[7]+	GND[7]	P0[7]-	P0[7]+
4	GND[6]	P3[6]-	P3[6]+	GND[6]	P2[6]-	P2[6]+	GND[6]	P1[6]-	P1[6]+	GND[6]	P0[6]-	P0[6]+
5	GND[5]	P3[5]-	P3[5]+	GND[5]	P2[5]-	P2[5]+	GND[5]	P1[5]-	P1[5]+	GND[5]	P0[5]-	P0[5]+
6	GND[4]	P3[4]-	P3[4]+	GND[4]	P2[4]-	P2[4]+	GND[4]	P1[4]-	P1[4]+	GND[4]	P0[4]-	P0[4]+
7	GND[3]	P3[3]-	P3[3]+	GND[3]	P2[3]-	P2[3]+	GND[3]	P1[3]-	P1[3]+	GND[3]	P0[3]-	P0[3]+
8	GND[2]	P3[2]-	P3[2]+	GND[2]	P2[2]-	P2[2]+	GND[2]	P1[2]-	P1[2]+	GND[2]	P0[2]-	P0[2]+
9	GND[1]	P3[1]-	P3[1]+	GND[1]	P2[1]-	P2[1]+	GND[1]	P1[1]-	P1[1]+	GND[1]	P0[1]-	P0[1]+
10	GND[0]	P3[0]-	P3[0]+	GND[0]	P2[0]-	P2[0]+	GND[0]	P1[0]-	P1[0]+	GND[0]	P0[0]-	P0[0]+

Serviceability – Hot-swap

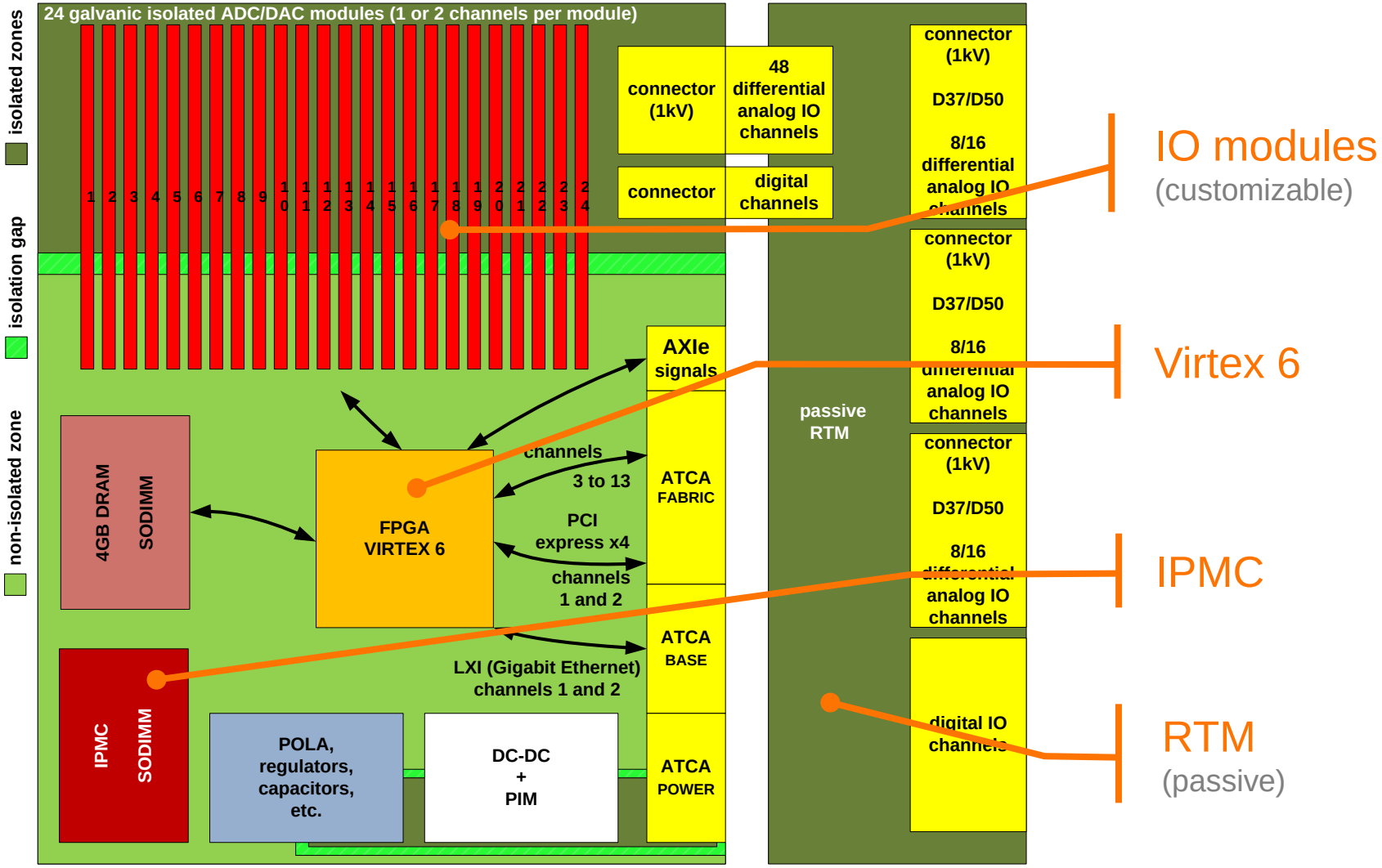


I/O

A system with I/O connectors on the back is more serviceable and improve maintenance:

- Easier cabling management.
- More functional card hot-swap.

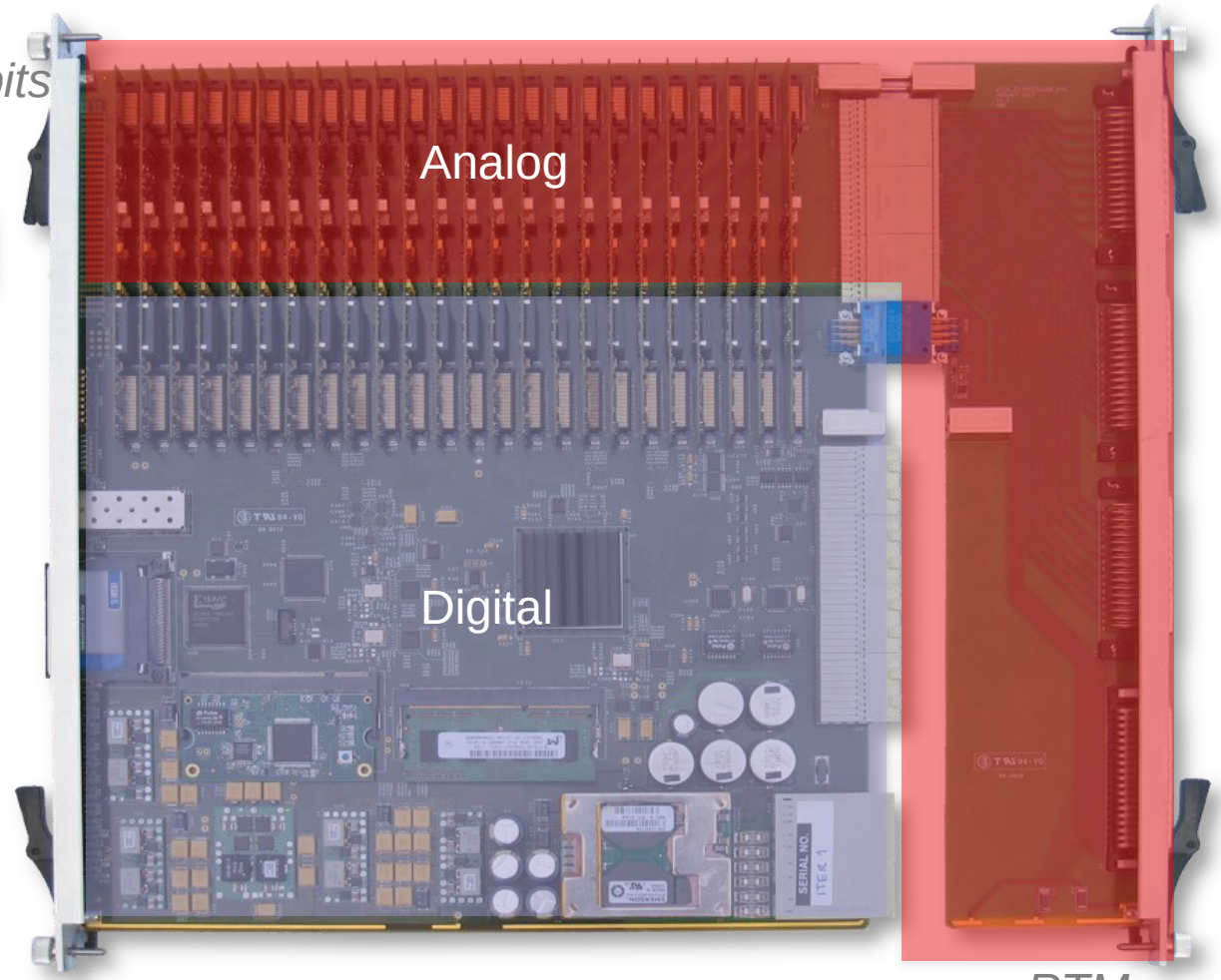
Modularity


isolated zones
isolation gap
non-isolated zone
24 galvanic isolated ADC/DAC modules (1 or 2 channels per module)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
connector (1kV)
48 differential analog IO channels
connector
digital channels
AXIe signals
ATCA FABRIC
ATCA BASE
ATCA POWER
4GB DRAM SODIMM
FPGA VIRTEX 6
channels 3 to 13
PCI express x4
channels 1 and 2
LXI (Gigabit Ethernet) channels 1 and 2
IPMC SODIMM
POLA, regulators, capacitors, etc.
DC-DC + PIM
passive RTM
connector (1kV) D37/D50 8/16 differential analog IO channels
connector (1kV) D37/D50 8/16 differential analog IO channels
connector (1kV) D37/D50 8/16 differential analog IO channels
digital IO channels
IO modules
(customizable)
Virtex 6
IPMC
RTM
(passive)

EMC Compatibility – Analog/Digital Separation

ADC module -1/2MSPS, 18 bits
with ADC x2 and chopper mode

DAC module
with DAC x2



RTM
Passive

B. Timing Extensions for ATCA (PDG.0)

B. ATCA Precision Timing Distribution

- A timing distribution system to use extended options lines or added special lines in the ATCA backplane for higher precision.
  - Harmonize and add Clocks, Gates & Triggers/Time-stamp (CGT) resources;
  - Guideline for users in which the specific implementation for most applications can be accomplished within the base ATCA 3.0 specification (to avoid re-design current backplanes);
  - Keep the concept that a timing source in any slot may drive any other slot.
  - Possibility of considerably higher precision with modifications to the backplane.
- Improve the compatibility between µTCA and ATCA platforms.
- Currently as draft guidelines PDG.0

ATCA timing resources

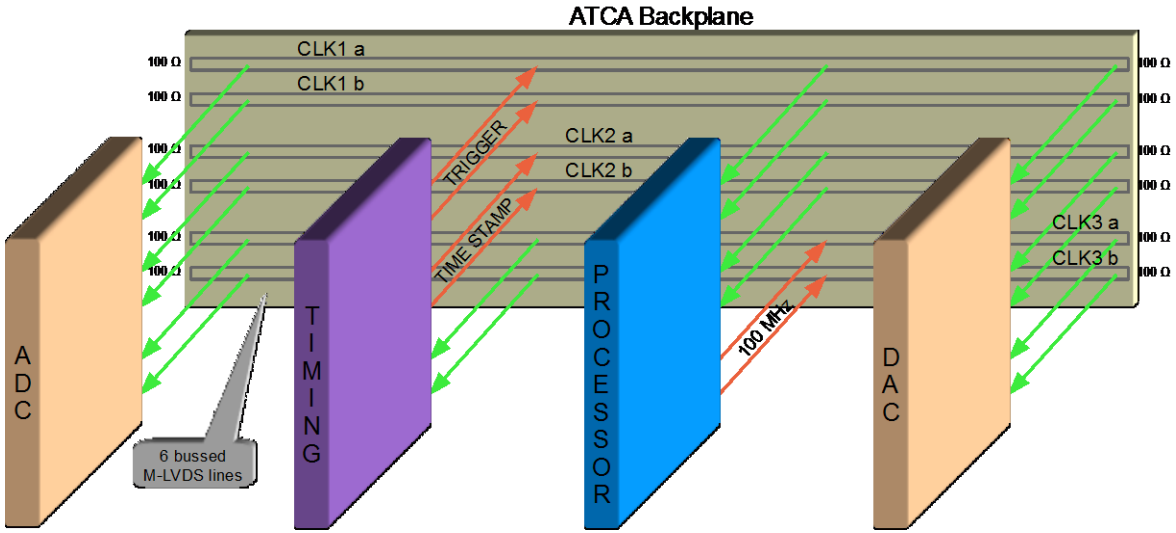
The following slides will present:

- An overview of resources for Clock Interfaces on ATCA.

A. Synchronization Clock Interface
B. Base Interface
C. Fabric Interface
D. Shared Fabric Interface
E. Fabric Interface (Clock Hub)
F. Update channel interface
G. Midplane clock interface

- Examples of implementation.

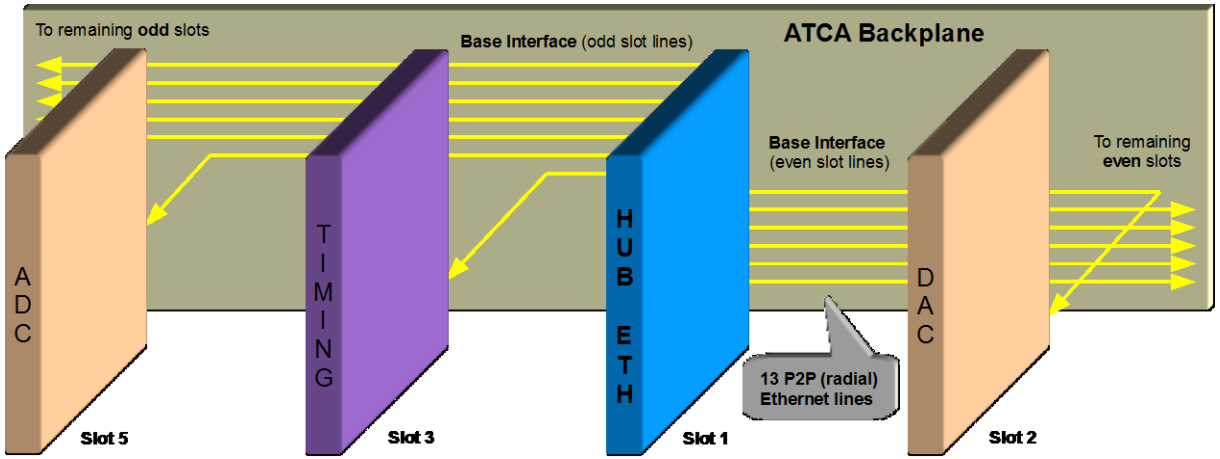
A. Synchronization Clock Interface

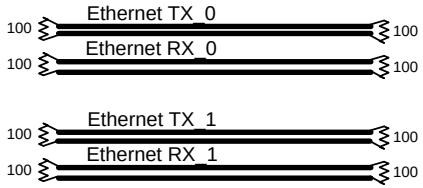


- Provides separate CGT signals → keeps full data bandwidth on fabric on ALL slots (even for full-mesh).

Interface	CLK1, CLK2, CLK3 (a,b)
CGT signals available	■ 6 (or 3 redundant) ■ CGT signals ■ Time-stamp signals
Performance	■ Fair ■ Bused ■ 100 MHz
ATCA 3.x Compatible?	■ Yes, fixed frequency CLK1 (8 kHz) and CLK2 (19.44 MHz) changed to user-defined
CGT signals on fabric	■ No
Issues	■ No radial CGT signals ■ Limited frequencies ■ Slot-to-slot skew not deterministic

B. Base Interface

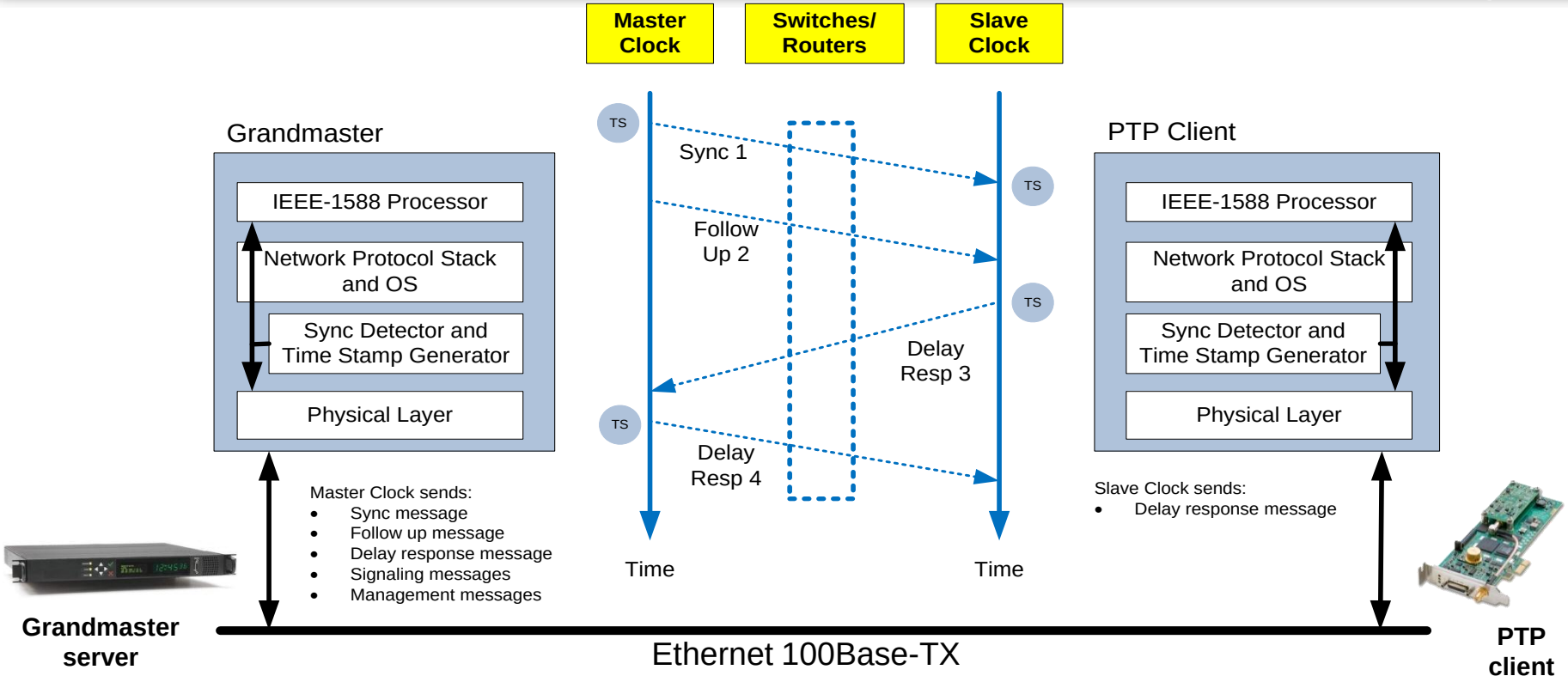




- Compatible to dual-star backplanes.
- Allows timing redundancy.
- Can be used as complementary or substitute of a specific clock hub.

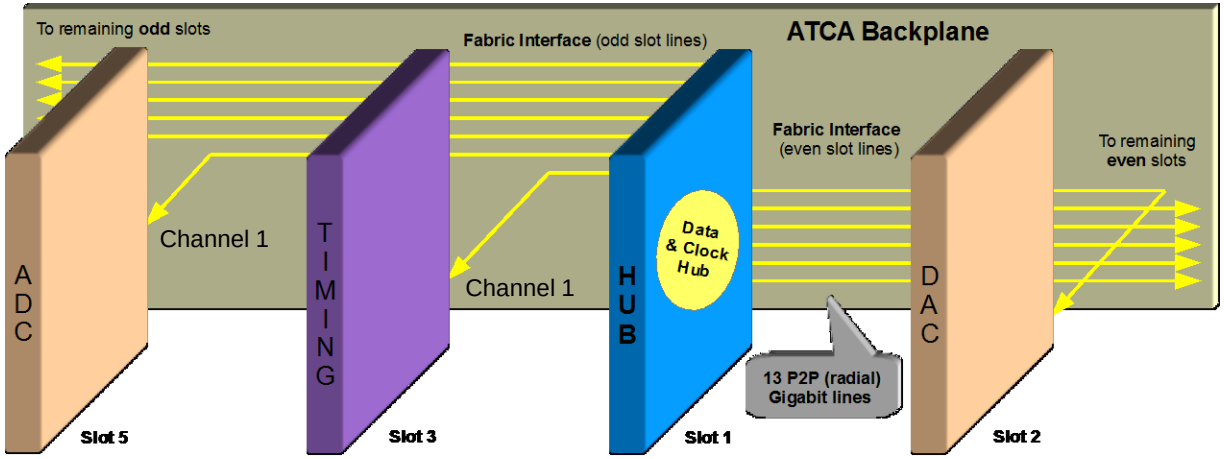
Interface	Ethernet ports from hub in Slot 1 (redundant on Slot 2)
CGT signals available	None. IEEE-1588 time encoded on 10/100/1000BASE-T
Performance	Good (P2P) ■ ~0.2GHz ■ < 50ns jitter (IEEE-1588)
ATCA 3.x Compatible?	■ IEEE-1588: yes ■ White-Rabbit: no (incompatible to 10/100/1000BASE-T)
CGT signals on fabric	None
Issues	■ Timestamps only ■ High skew/jitter

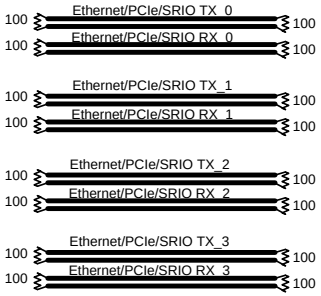
IEEE-1588 (PTP)



- Precision Time Protocol (PTP) is a protocol used to synchronize clocks throughout a computer network.
- Master-slave architecture where master is elected (best precision).
- Time synchronization accuracy < 40 ns RMS.

C. Fabric Interface (Communications Protocol)



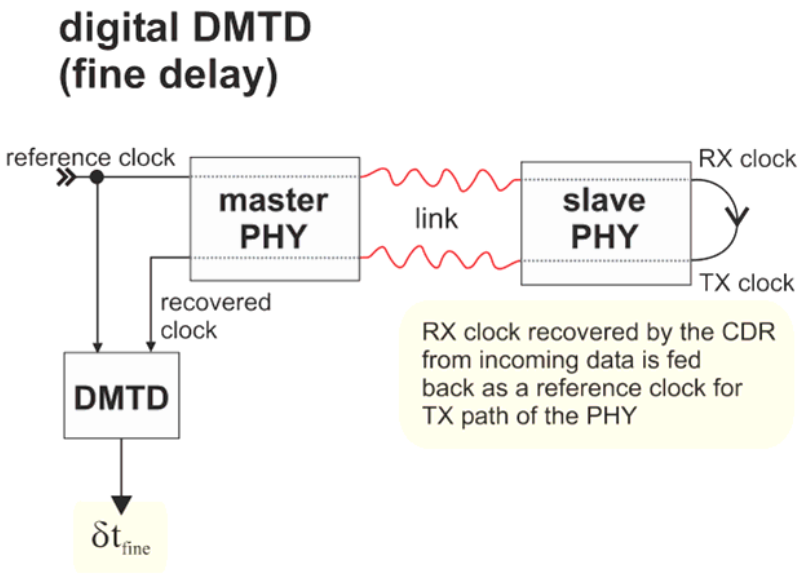


- 10GBASE-KR (10.3125 Gbit/s, 64B/66B) (and a 40GBASE-KX4) will allow better accuracies.

Interface	Ethernet/PCIe/SRIO hub in Slot 2, (redundant in Slot 2)
CGT signals available	None. Time encoded on: ❑ Ethernet 1000BASE-BX or 10GBASE-BX4: ❑ IEEE-1588 ❑ White-Rabbit ❑ PCIe/SRIO: unknown
Performance	Good* (P2P) ❑ <100 ps jitter (White-Rabbit)
ATCA 3.x compatible?	Compatible
CGT signals on fabric	None
Issues	❑ Time-stamps only ❑ High skew/jitter of IEEE-1588

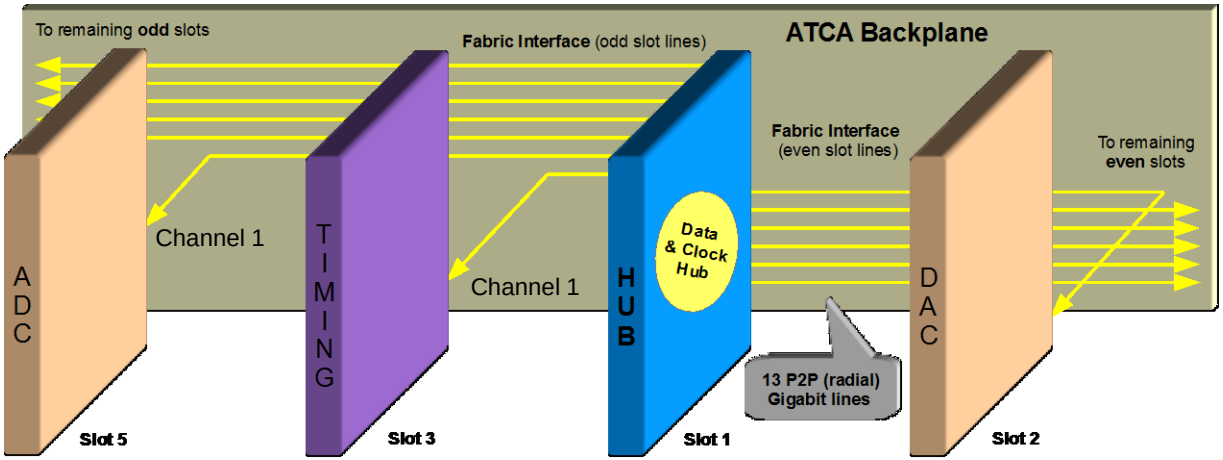
White Rabbit

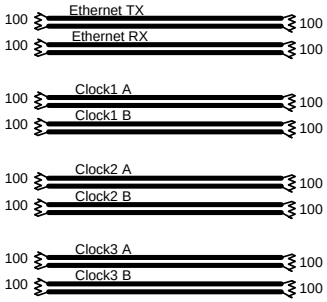
- Compatible to the IEEE-1588-2008 specification.
- All nodes receive a synchronous physical layer clock:
  - Generated by the Grand-master (125 MHz, 8 ns period).
  - Encoded at the transmitter PHY and recovered in the receiver PHY.
- Uses hardware-assisted PTP for clock synchronization
  - Synchronizes local clock with the master clock by measuring and compensating the **coarse delay**.
  - **Fine delay** adjustment use a digital 'Dual Mixer Time Difference' phase comparator.



❑±350 ps skew accuracy over 5 km fiber point-to-point link.

D. Shared Fabric Interface



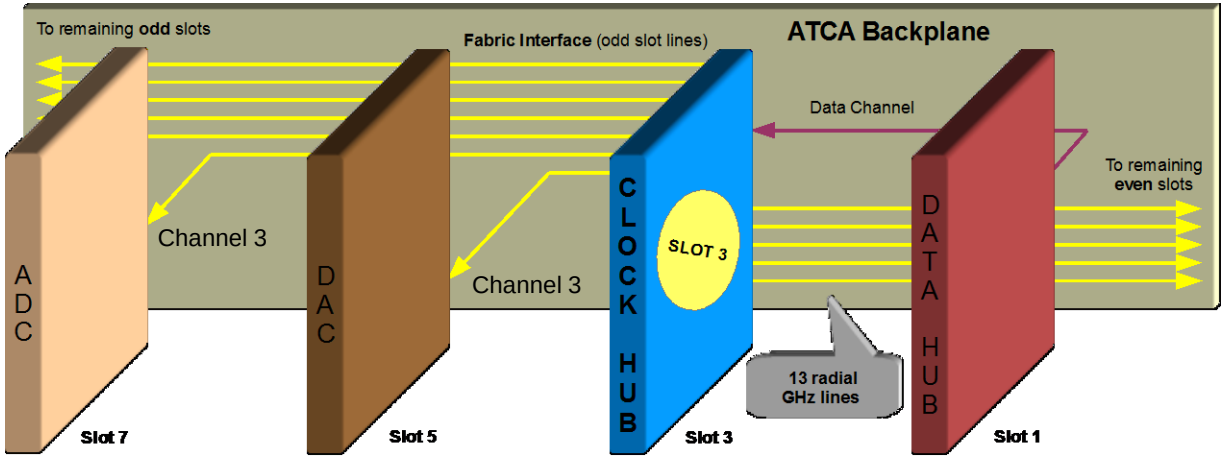


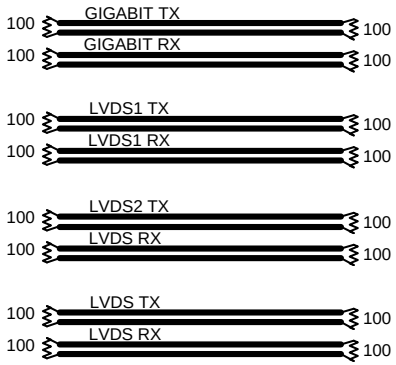
- Can be used on all fabric configurations (even full-mesh).

Interface	❑ Hub in Slot 1(2) ❑ Timing and Data lines share a fabric channel
CGT signals available	All nodes can receive/send ≤ 6 (3 redundant) CGT signals
Performance	Good* (P2P) ❑ ~3 GHz ❑ <100 ps jitter
ATCA 3.x compatible ?	❑ New definition ❑ New Hubs/Nodes ❑ Data rate:1x 2x ~~4x~~
CGT signals on fabric	Yes
Issues	❑ Limits data throughput ❑ Less CGT signals

* Can be further improved on backplanes re-designed for low crosstalk noise and equal length lines.

E. Fabric Interface (Clock Hub)





- Compatible with both dual-dual star and full-mesh backplanes.
- Provides separate CGT signals → keeps full data bandwidth on fabric channels.

Interface	❑ Clock Hub in Slot 3, (redundant: 4) ❑ Node cards use Channel 3, (or redundant: 4)
CGT signals available	All nodes can receive/send ≤ 8 (≤ 4 redundant) CGT signals
Performance	Good* (P2P) ❑ ~3 GHz ❑ <100 ps jitter
ATCA 3.x compatible?	Compatible
CGT signals on fabric	Yes
Issues	❑ Channel 3 in Slots 1(2) reserved for data ❑ Clock Hub can't participate on full-mesh data network

* Can be further improved on backplanes re-designed for low crosstalk noise and equal length lines

Fabric interface
Clock Hub on Slot 3(4)

- The Clock Hub uses fabric Channels 3-15 as radial bidirectional links to the node cards on Slots 4-16.
- The Clock Hub implements the following functions:
  - local generation of clock signals and distribute it to the node cards.
  - route timing signals from/to node cards (broadcast, multicast or P2P).

The following types of signals are defined:

Name	Code	Signal type	Description
BST	1h	Binary State Timing	clock, gate and trigger binary type signals
WET	2h	Word encoded BST	synchronous time multiplexed BST signals on a ‘n’-bit word (e.g. 8b/10b -> n = 8 signals)
MET	3h	Message encoded Timing	▪ Deterministic timing messages (sequence of words) modulated on a carrier clock. ▪ Carry trigger/event signals transport, clock skew correction, and time stamp
TSS	4h	Time-stamp signal	Serial one-line time information such as IRIG-B.

Dual dual-star backplane connections

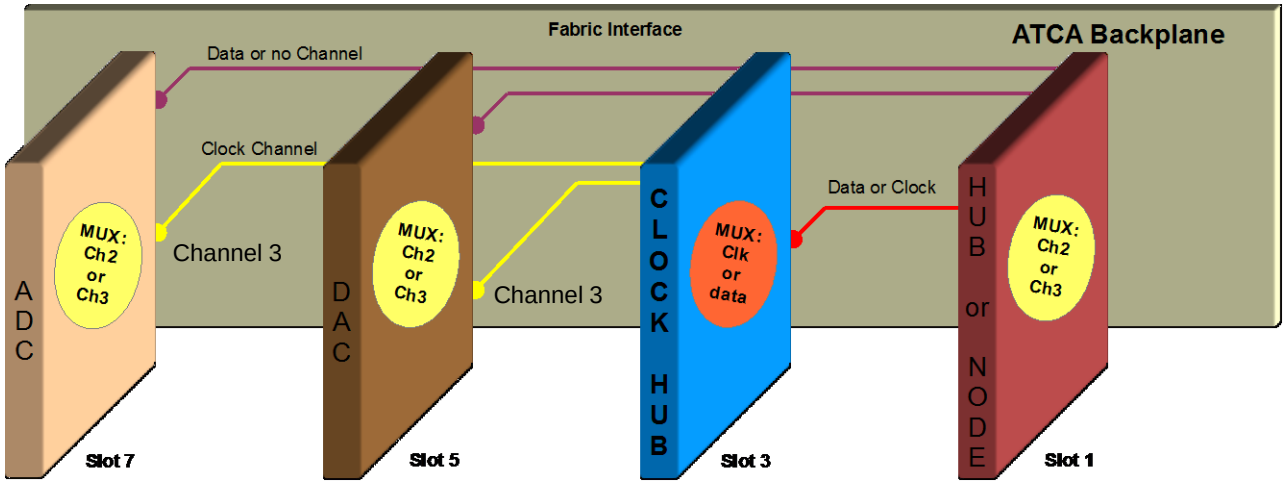
Logical Slot #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Plug	Ch																
P20	15	16-1	16-2	16-**3**	16-**4**												
P20	14	15-1	15-2	15-**3**	15-**4**												
P20	13	14-1	14-2	14-**3**	14-**4**												
P21	12	13-1	13-2	13-**3**	13-**4**												
P21	11	12-1	12-2	12-**3**	12-**4**												
P21	10	11-1	11-2	11-**3**	11-**4**												
P21	9	10-1	10-2	10-**3**	10-**4**												
P21	8	9-1	9-2	9-**3**	9-**4**												
P22	7	8-1	8-2	8-**3**	8-**4**												
P22	6	7-1	7-2	7-**3**	7-**4**												
P22	5	6-1	6-2	6-**3**	6-**4**												
P22	4	5-1	5-2	5-**3**	5-**4**	4-4	4-5	4-6	4-7	4-8	4-9	4-10	4-11	4-12	4-13	4-14	4-15
P22	3	4-1	4-2	4-**3**	3-**3**	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11	3-12	3-13	3-14	3-15
P23	2	3-1	3-2	2-**2**	2-**3**	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
P23	1	2-1	1-1	1-**2**	1-**3**	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	1-12	1-13	1-14	1-15

(SLOT-CHANNEL)

Row #	Interface Designation	J22/P22 Connector Pairs (Node board)			
		ab	cd	ef	gh
9	Fabric Channel 3	BST_Tx2[3]	BST_Rx2[3]	BST_Tx3[3]	BST_Rx3[3]
10		**xET_Tx[3]**	**xET_Rx[3]**	BST_Tx1[3]	BST_Rx1[3]

4x Channel
(8 diff pairs)

When use Clock Hub on Slot 3?



This type of Clock Interface shall be used when:

- Fabric Data Hub inserted in Slot 1.

  and

- Fabric Clock hub on Slot 3 require fabric data connections (e.g. PCIe for board setup)

- IF the channel toward Slots 1 may not be not used for data, then:

  Clock Hub on Slot 3:

  - May include a bidirectional multiplexer to select between outbound clock signals or inbound data signals on Channel 1 and 2;
  - Shall provide the clock interface on Channels 3 to 15 as usual;

  Node boards shall include a bidirectional multiplexer to select the:

  - Clock interface from Channel 3, if the node board is inserted in Slot 4 to 16;
  - Clock interface from Channel 2, if the node board is inserted in Slot 1 or 2.

Clock Interface Port configuration

Checked by the HMU

Table A Port Signal Levels

Code 1 Byte	Signal type
1h	LVDS (differential)
2h	MLVDS (differential)
3h	CML (differential)
4h	LVECL (differential)
5h	LVPECL (differential)
6h-31h	reserved
32h-63h	OEM

Table B Port Signalling

Code 1Byte	Protocol
1h	BST
2h	WET
3h	MET
4h	TSS
4h-31h	reserved
32h -63h	OEM

Port Configuration example:

Port 0	Port 1	Port 2	Port 3
MET	CLOCK		
WET	CLOCK	CLOCK	TSS
MET	CLOCK	TRIGGER	GATE
MET	CLOCK	TRIGGER	TSS
WET	CLOCK	TRIGGER	TSS

MET signaling options:

- PICMG 3.1 Ethernet
- PICMG 3.4 PCI Express
- PICMG 3.5 Serial RapidIO

WET signaling options:

- 8b10b, 64b66b

TSS signaling options:

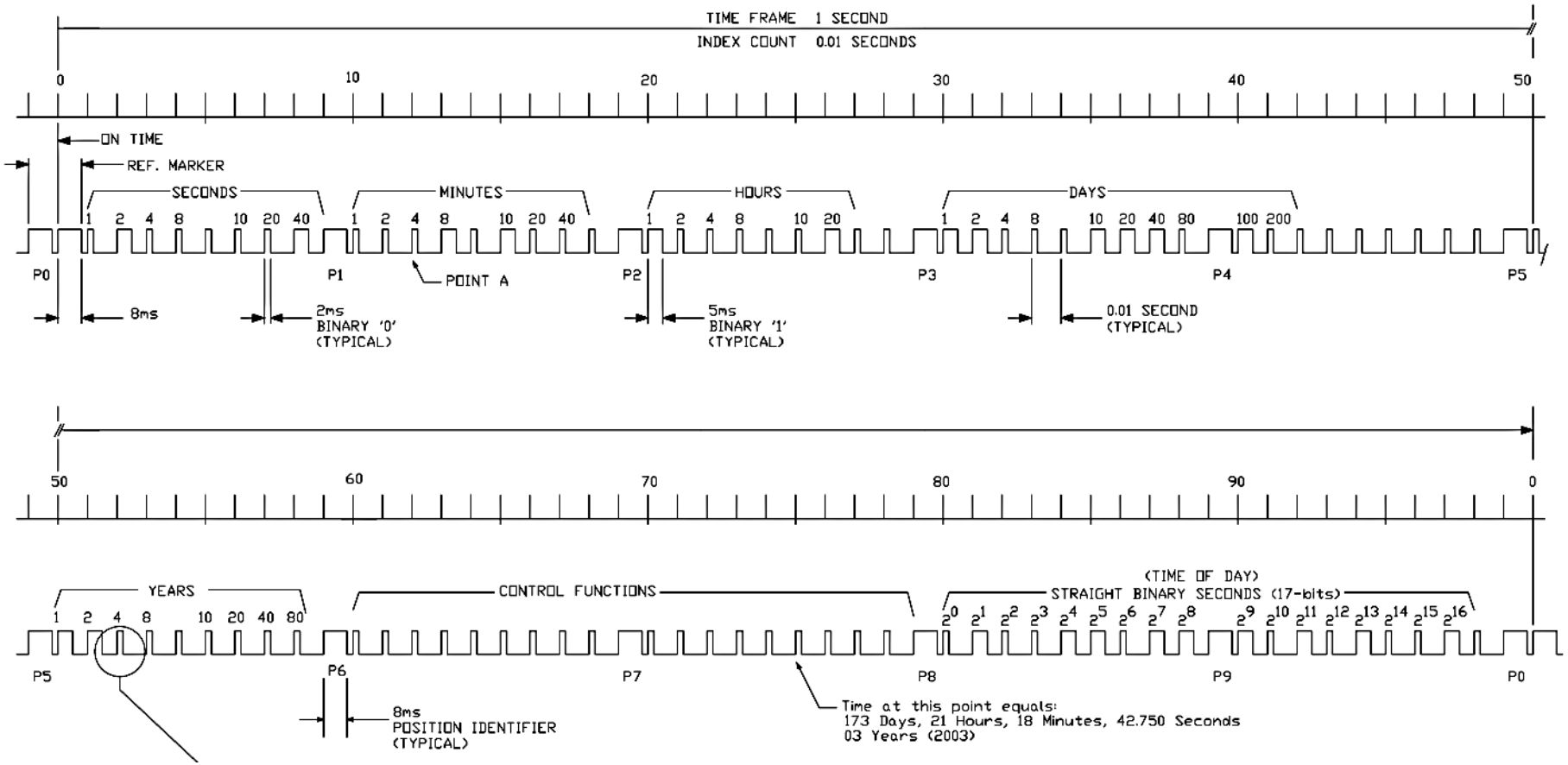
- IRIG-B Direct Current Level Shift – DCLS (width coded) over LVDS.

MET protocols

Performance criteria: time jitter and channel to channel skew

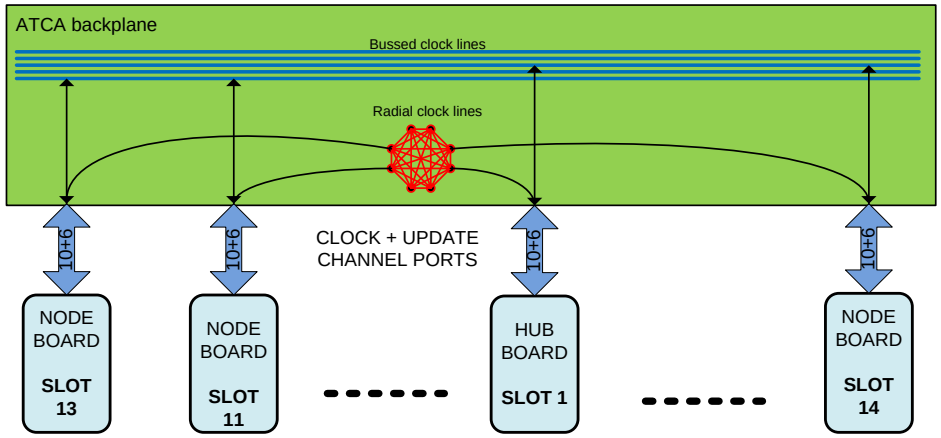
- Proprietary (e.g. using FPGA)
  - Can be tailored for maximum synchronization performance.
  - Higher level synchronization protocols (PTP) and link delay compensation (down to *ps*) can be straightforwardly added.
  - Example: DESY system wide synchronization (µTCA) for XFEL.
- IEEE-1588 or White Rabbit over Ethernet
- WR-like protocol over PCIe or SerialRapidIO?
  - Expected even lower time jitter.
  - Synchronous → link delay compensation can be added.

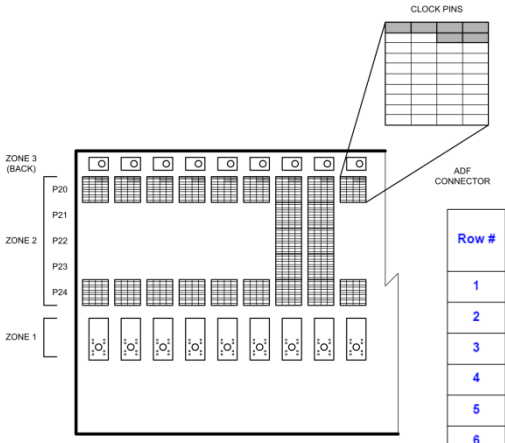
Inter-Range Instrumentation Group (IRIG) time codes



Format B: BCD time-of-year in days, hours, minutes, seconds and year and straight binary seconds-of-day and control bits.

F. Update Channel Interface



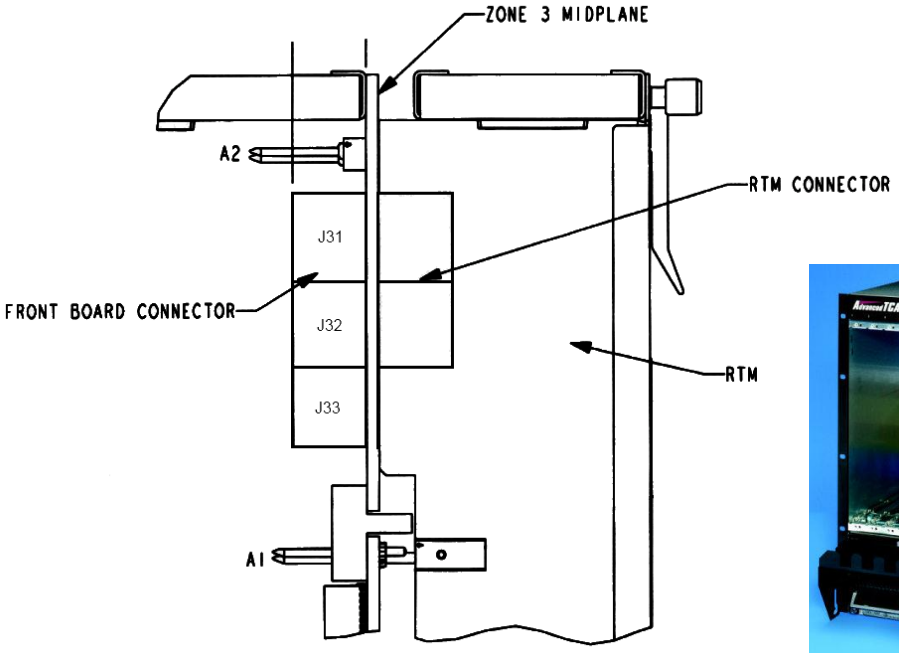


Row #	Interface Designation	J20/P20 Connector Pairs							
		a b		c d		e f		g h	
1	Clks	CLK1A+	CLK1A-	CLK1B+	CLK1B-	CLK2A+	CLK2A-	CLK2B+	CLK2B-
2	Update Channel & Clks	Tx4(UP)+	Tx4(UP)-	Rx4(UP)+	Rx4(UP)-	CLK3A+	CLK3A-	CLK3B+	CLK3B-
3		Tx2(UP)+	Tx2(UP)-	Rx2(UP)+	Rx2(UP)-	Tx3(UP)+	Tx3(UP)-	Rx3(UP)+	Rx3(UP)-
4		Tx0(UP)+	Tx0(UP)-	Rx0(UP)+	Rx0(UP)-	Tx1(UP)+	Tx1(UP)-	Rx1(UP)+	Rx1(UP)-
5	Fabric Channel 15	Tx2[15]+	Tx2[15]-	Rx2[15]+	Rx2[15]-	Tx3[15]+	Tx3[15]-	Rx3[15]+	Rx3[15]-
6		Tx0[15]+	Tx0[15]-	Rx0[15]+	Rx0[15]-	Tx1[15]+	Tx1[15]-	Rx1[15]+	Rx1[15]-
7	Fabric Channel 14	Tx2[14]+	Tx2[14]-	Rx2[14]+	Rx2[14]-	Tx3[14]+	Tx3[14]-	Rx3[14]+	Rx3[14]-
8		Tx0[14]+	Tx0[14]-	Rx0[14]+	Rx0[14]-	Tx1[14]+	Tx1[14]-	Rx1[14]+	Rx1[14]-
9	Fabric Channel 13	Tx2[13]+	Tx2[13]-	Rx2[13]+	Rx2[13]-	Tx3[13]+	Tx3[13]-	Rx3[13]+	Rx3[13]-
10		Tx0[13]+	Tx0[13]-	Rx0[13]+	Rx0[13]-	Tx1[13]+	Tx1[13]-	Rx1[13]+	Rx1[13]-

Interface	Ports of the Update Channel redefined for CGT signals
CGT signals available	Up to 10 signals per Slot (mix of full-mesh and bused signals possible)
Performance	Excellent # ❑ Low skew ❑ Low jitter
ATCA 3.x compatible ?	Not compatible with current designs using the Update Channel
CGT signals on fabric	No
Issues	Requires a new re-designed backplane

On backplanes designed for low crosstalk noise and equal length lines.

G. Zone 3 backplane Clock Interface

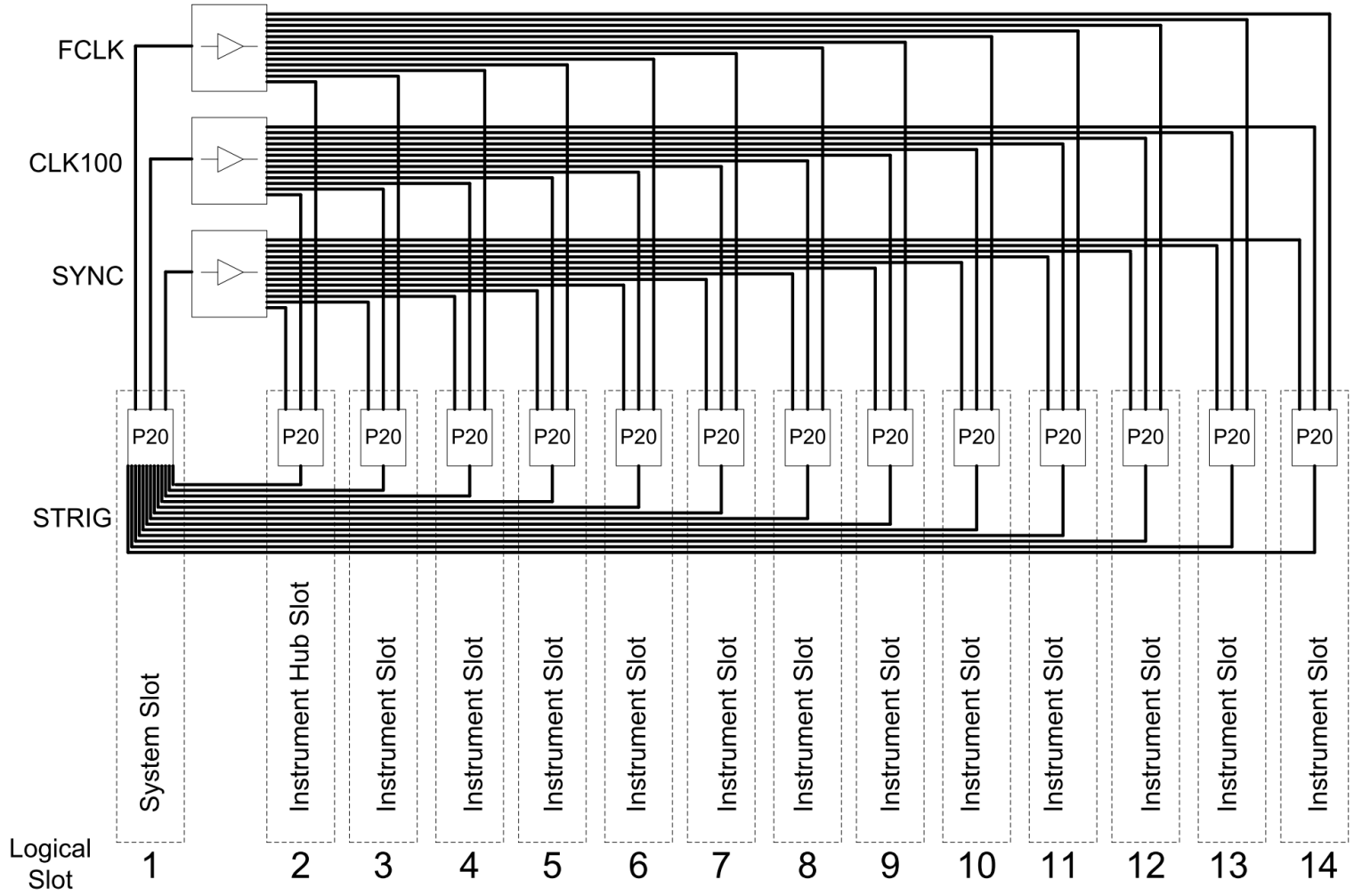


- Provides separate CGT signals → keeps full data bandwidth on fabric on ALL slots (even for full-mesh).
- Full-mesh or dual-star clock interface plus bussed clocks can be implemented.

Interface	Clock Ports on J33 of Zone 3 (RTM)
CGT signals available	❑ Full-mesh of CGT signals (2 line channels) ❑ 14 bused lines
Performance	Excellent # ❑ Low skew ❑ Low jitter
ATCA 3.x compatible?	Compatible
CGT signals on fabric	No
Issues	❑ Cost increase ❑ less I/O (just J31, J32) ❑ less area on RTM card

On backplanes designed for low crosstalk noise and equal length lines.

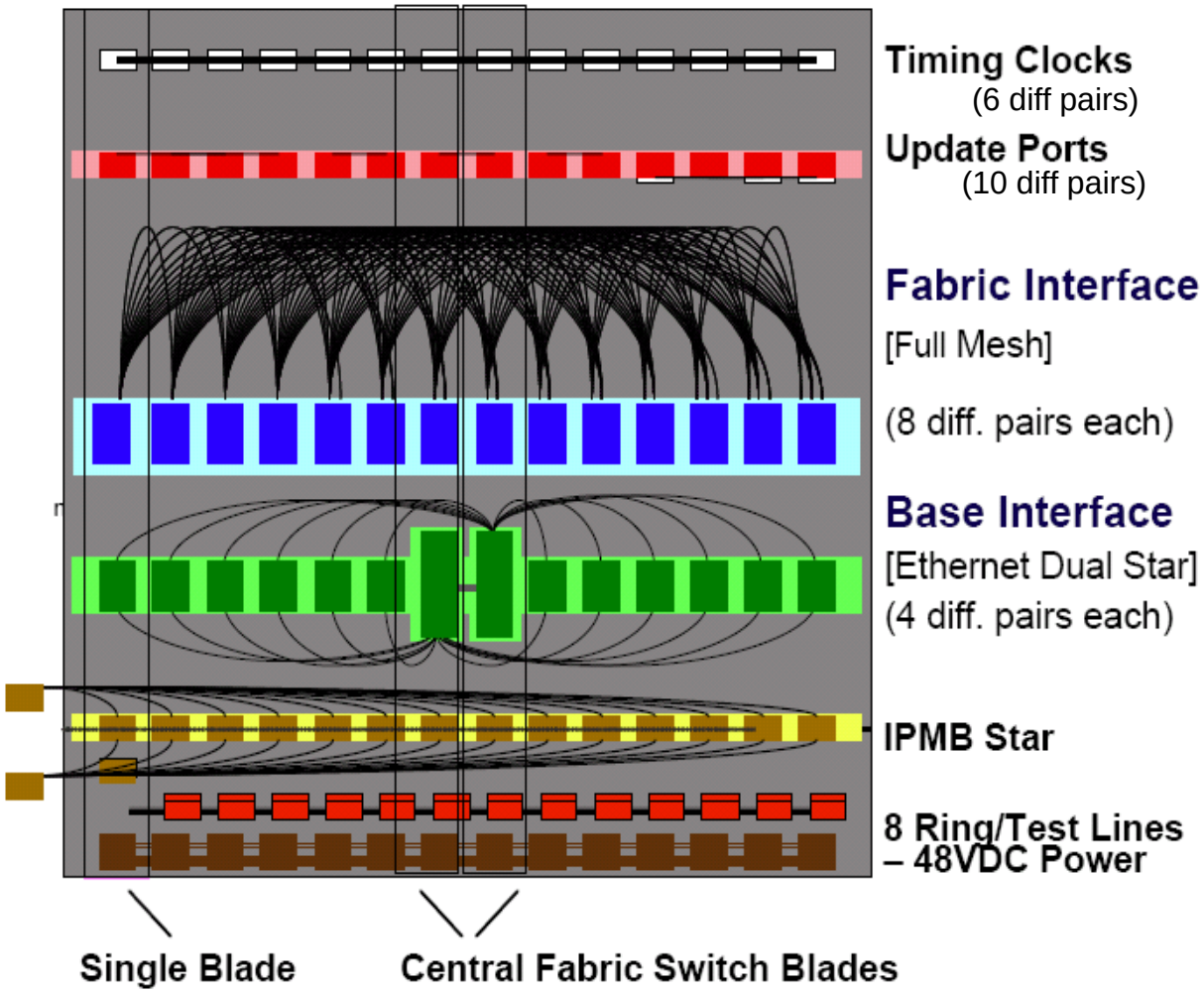
AXIe Timing Interface



CLOCK and UPDATE interface

AdvancedTCA backplane

- AdvancedTCA Data Transport
  - Differential signaling capable of 10 Gbps (XAUI) today
  - 5+ Gbps differential signal capacity
  - Single backplane supports many fabric technologies and topologies
- Base Interface
  - 10/100/1000 BASE-T Ethernet
  - Dual Star fabric topology
- Fabric Interface
  - SERDES (3.125 Gbps minimum)
  - 1x, 2x, or 4x Channels
  - Star or Mesh fabric topology
- Synchronization Interface
  - Three dedicated clock interfaces (8kHz, 19.44 MHz, user defined)
  - Redundant buses
- Update Channel
  - Point to point connection between two slots



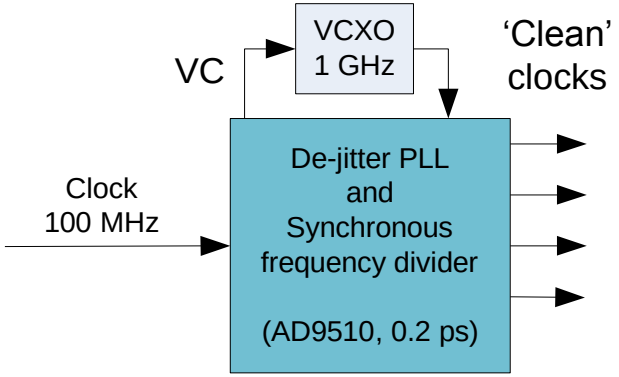
xTCA v. AXIe timing

Function	AXIe	xTCA Fabric Hub Slot 3
Star timing signals	3 unidirectional and 1 bidirectional pairs per slot	6 bidirectional pairs per slot
MET or WET signals	-	One x1 port (2 pairs up to 5 Gbit/s) per slot*
Bussed signals	12 pairs	6 pairs
Daisy-chained Local bus	2 x 8 pairs per slot	-
Update interface	-	10 pairs
Fabric Channel 14-15	-	16 pairs
Slots with timing signals (except Hubs)	2 to 14 (13)	5 to 14 (10) on 19” 5 to 16 (12) on 23”
Backplane length compensation	Length trimmed timing star traces	Use standard backplanes – automatically adjustable delay lines on timing hub if required

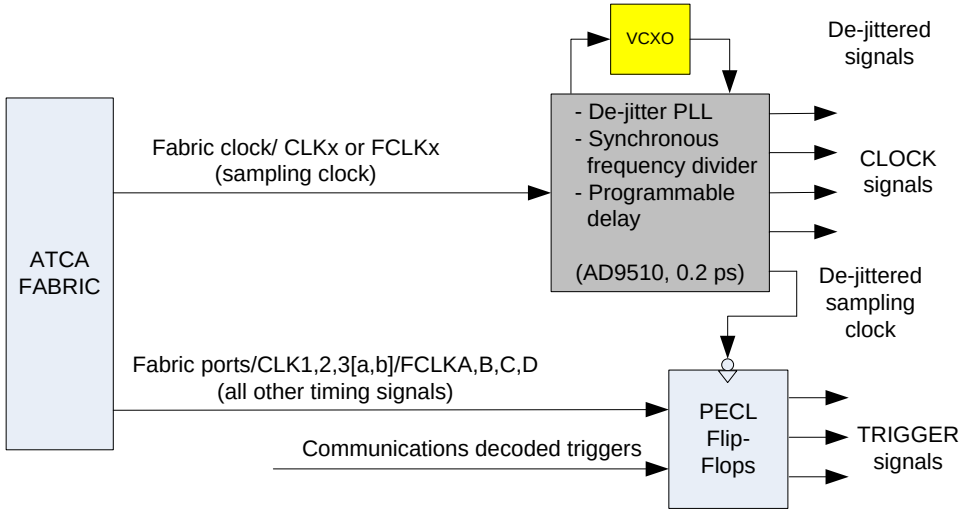
- Number of simultaneous WET signals depends on the time resolution, e.g. 8 signals @ 4 ns resolution, 32 signals @ 16 ns resolution … (for a signaling of 2.5 Gbit/s).
- MET are non-simultaneous event ocurrence messages with a timing resolution (time slot) depending on the message size, e.g. 32 ns for a 64-bit message (2.5 Gbit/s signaling) (2^64 distinct events when all bits are used for this purpose)..

CGT signal integrity

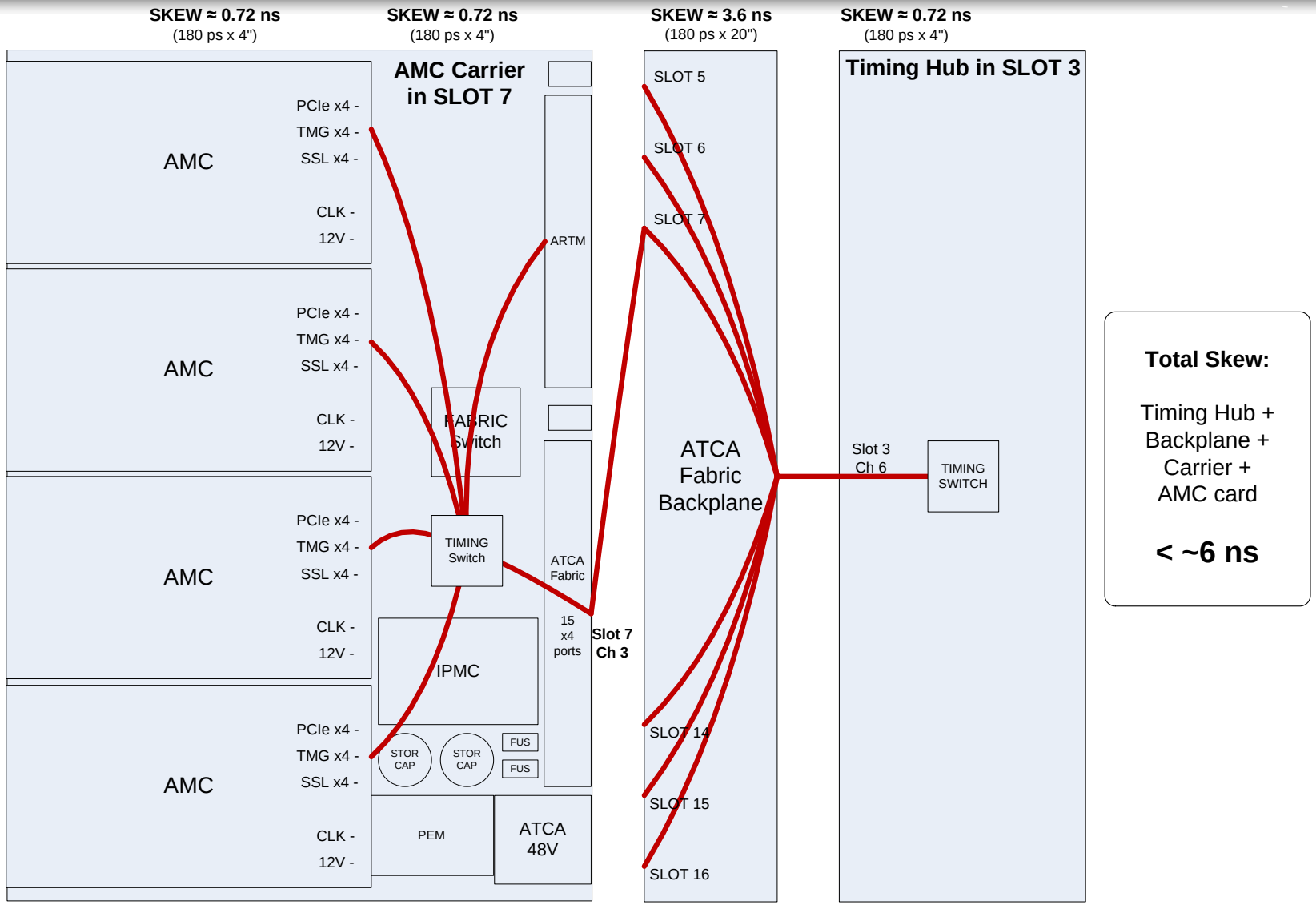
- Clock signals can be de-jittered using a PLL/VCXO de-jitter circuit
  - < 1ps achievable.
  - Fractional clocks can be obtained.



- CGT signals can be de-jittered by sampling it with a de-jittered clock.
  - A deterministic signal delay of ½ the clock period will be added.
  - Slight higher jitter than the sampling clock due to the addition of a flip-flop.
  - Sampling period must be smaller than the CGT signal smallest width (Nyquist).
  - Each clock domain signals requires one PLL.

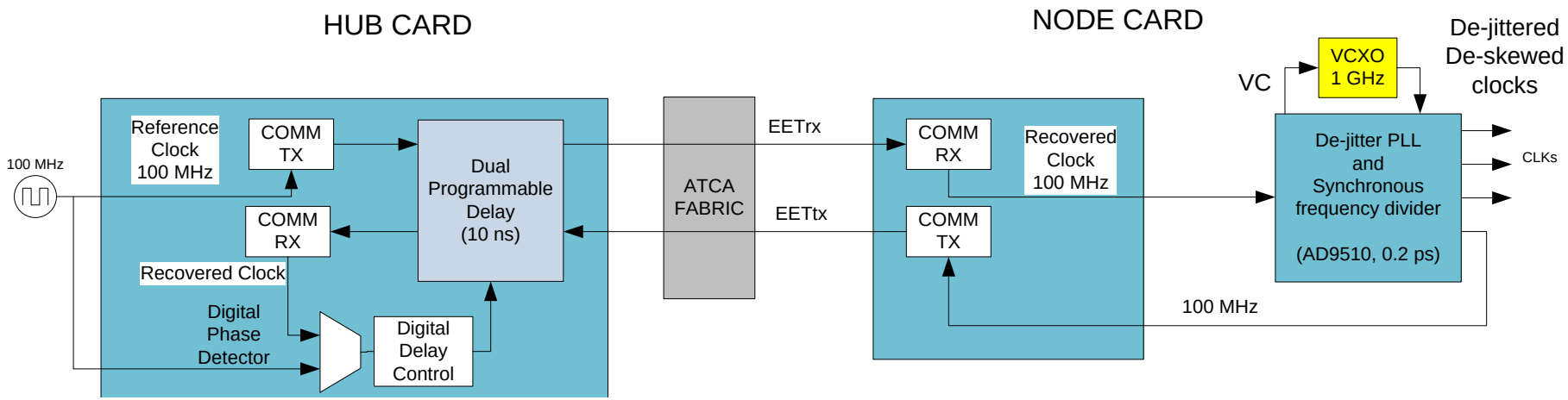


Timing Signals Skew



Skew Compensation

- Manual compensation
  - Programmable delay devices on all clock lines
- Automatic skew compensation
  - Uses a clock loop phase compensation on xET.
  - Matches the different propagation delays on all node cards (up to ~6 ns skew).
  - The RX path delay must designed to be similar to the TX path delay.
  - Both clock and xET decoded timing signals are de-skewed.
  - Clock de-jittering included by design.

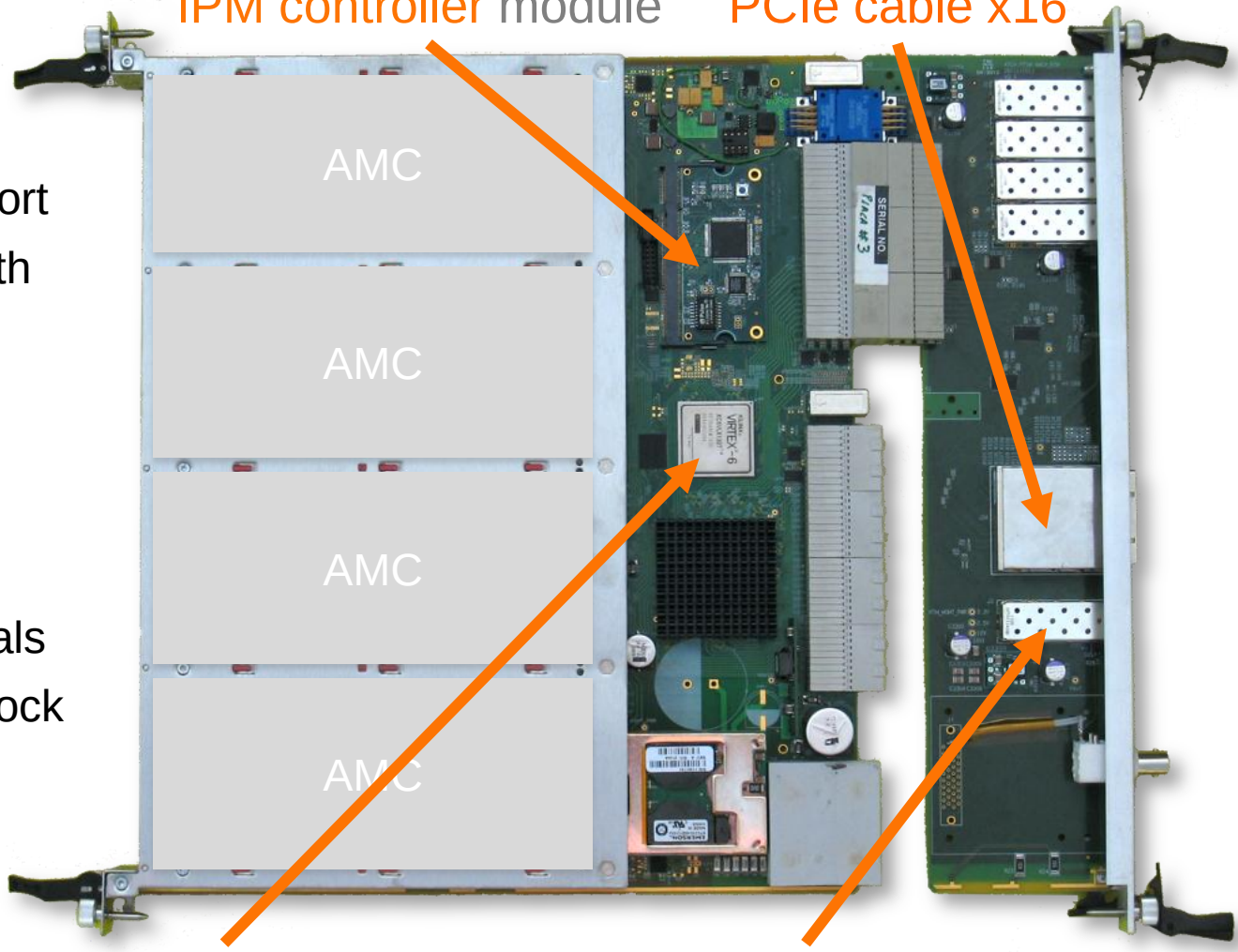


Simplified example of an automatic skew adjustment circuit.

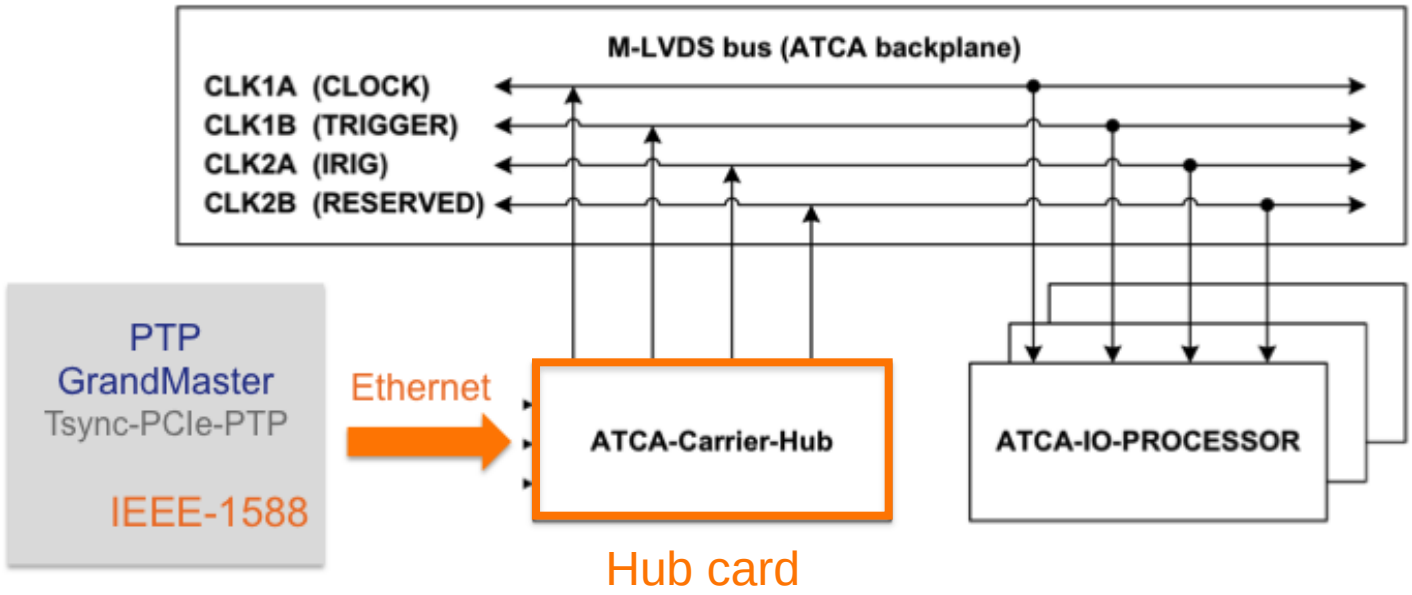
Example Implementations for ATCA/AMC carrier

ATCA AMC-Carrier / PCIe Hub / Timing Node

- IEEE-1588 or White-Rabbit Ethernet support
- Clock de-jitter PLL with servo
- Switch on FPGA for timing distribution
- IRIG-B encoding to backplane
- Decoded trigger signals
- Common 100 MHz clock to all cards

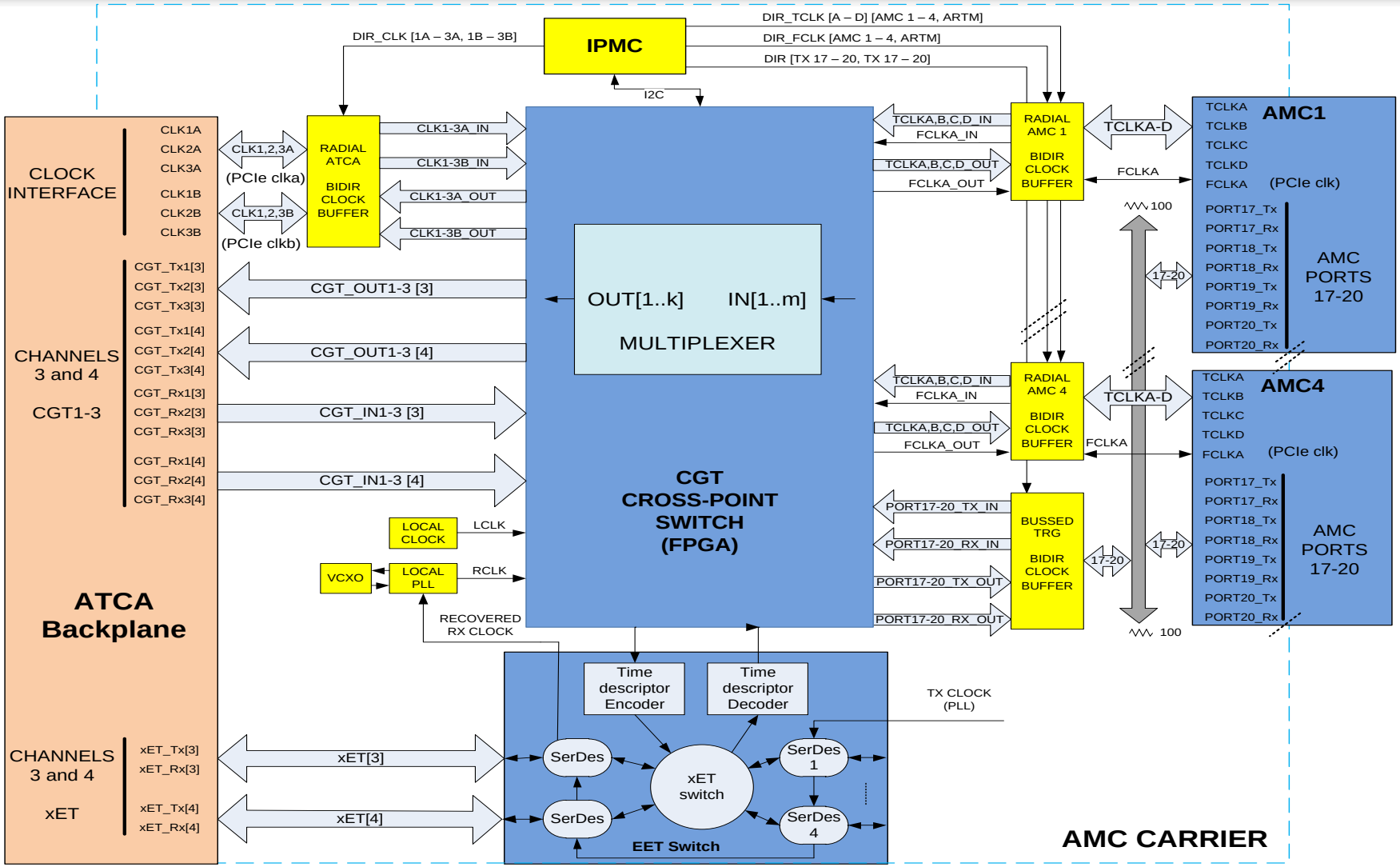


ATCA Synchronization Clock Interface Example (ITER FPSC)

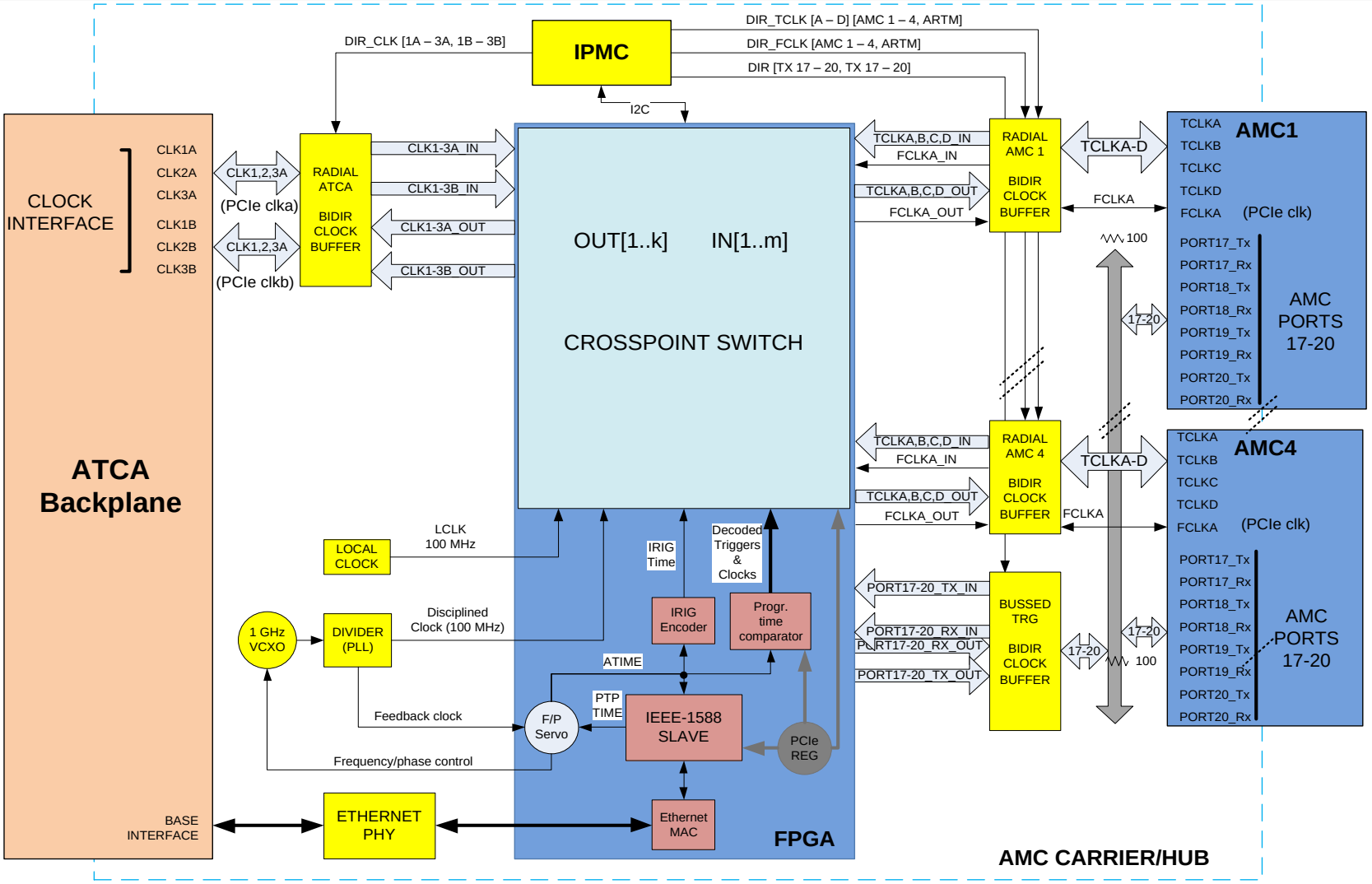


- Time stamping of acquired data using IRIG time distributed by hub card
  Internal time counter synchronized with IEEE-1588-2008.
- Programmable timing unit for generating specific clock or trigger sequences for sampling.

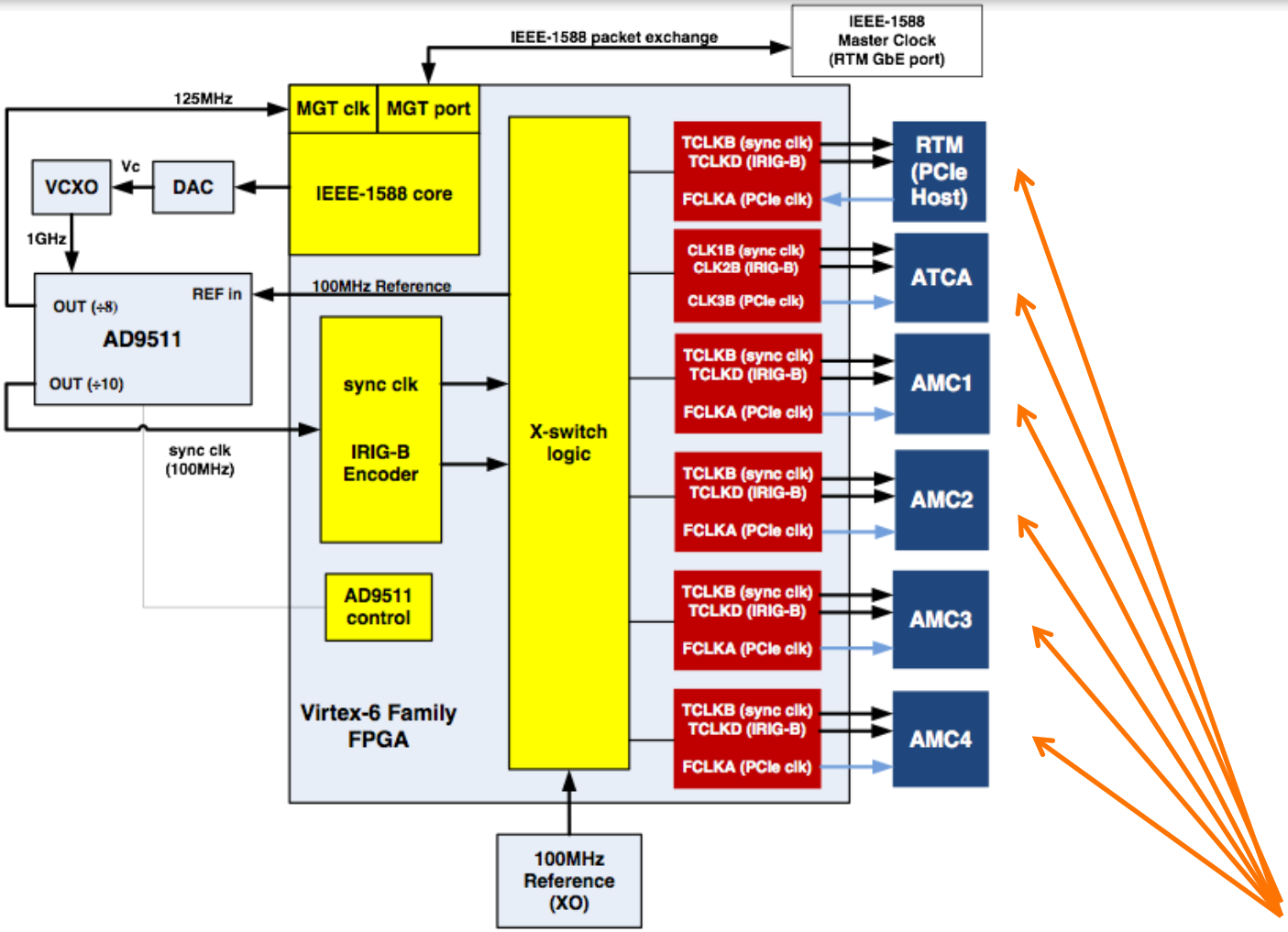
ATCA Fabric Clock Interface Example (AMC Carrier)



ATCA Base Interface example



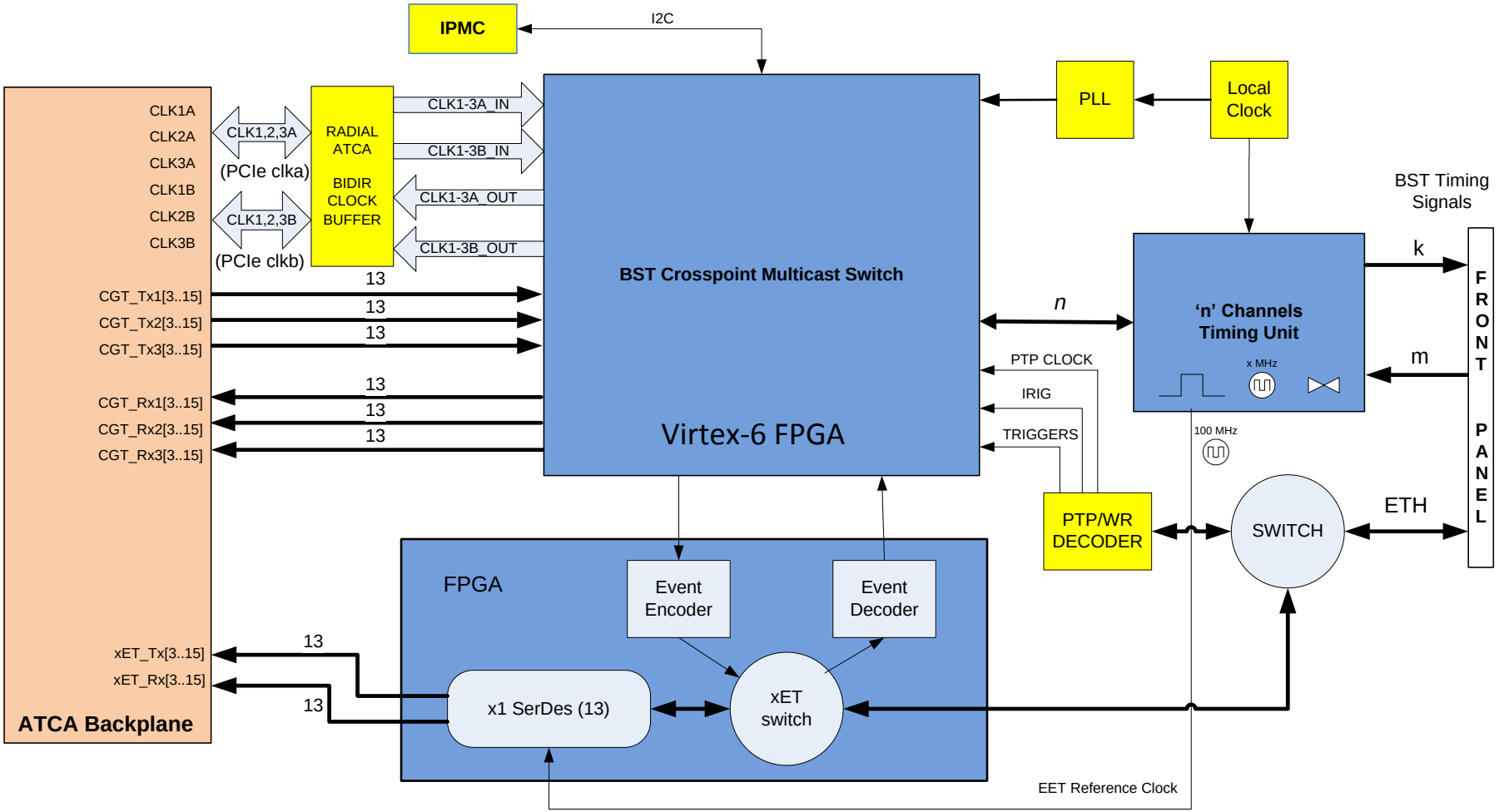
FPGA Timing Switch / Servo



Each clock signal source may be independently located

(on each of the AMC cards, RTM or ATCA backplane)

Timing Hub driving Fabric Interface Example

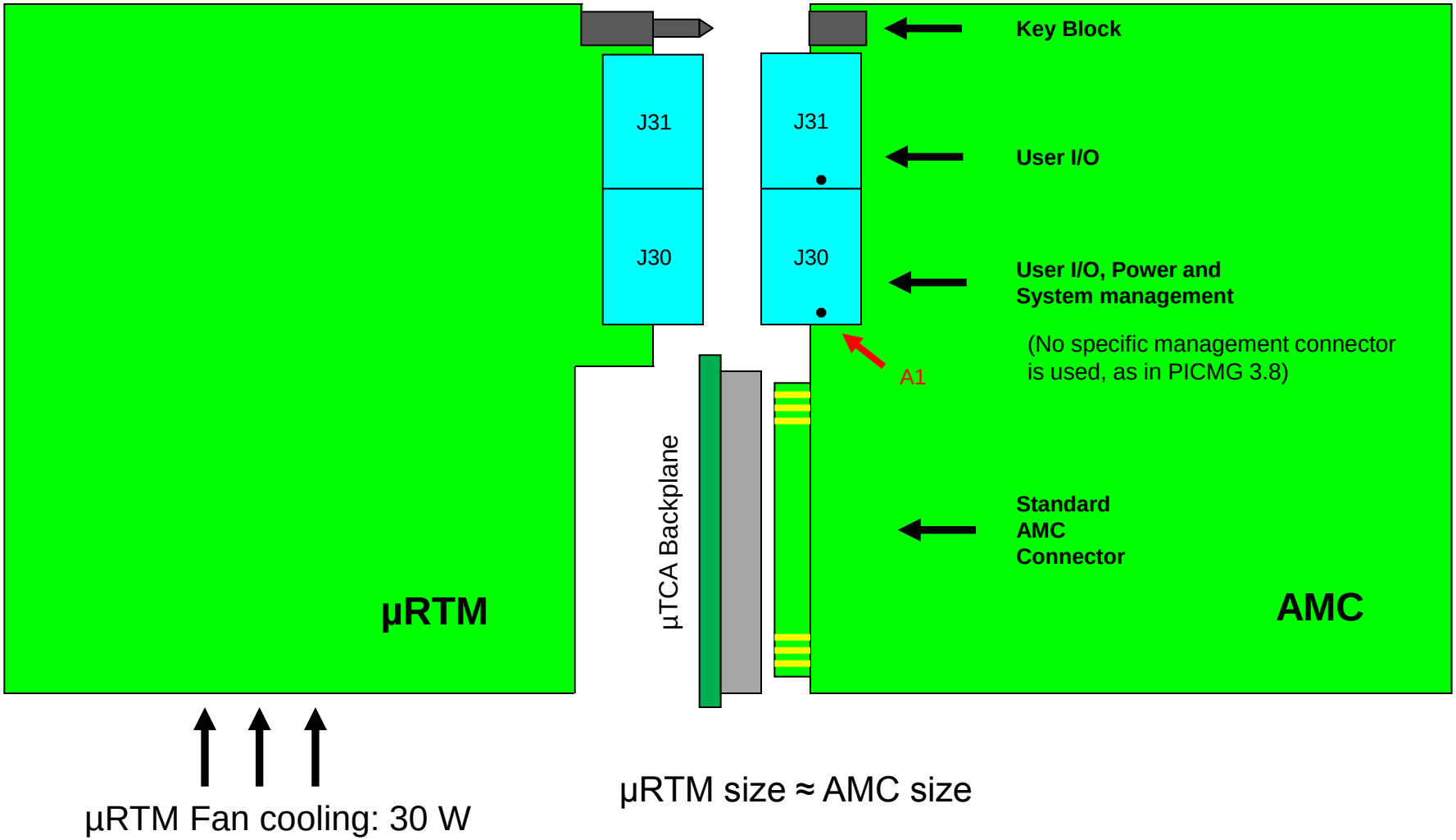


C. MicroTCA µRTM Extensions (MTCA.4)

C. MicroTCA µRTM Extensions (MTCA.4)

- The needs of the Physics community led to the development of standard specifications for Physics based on MicroTCA.
  - Double-wide AMC card and its mechanics (mostly µTCA is reused);
  - Companion double-wide µRTM card and interface (definitions for IO, power and IPMI management);
  - A new 12-slot MTCA shelf – the original Double Wide Shelf AMC shelf specified by PICMG didn't provide an RTM, although the module itself allowed a user-defined connector in the RTM area (Zone 3).

MTCA.4 double size AMC and µRTM (component side)



µRTM User I/O (J31)

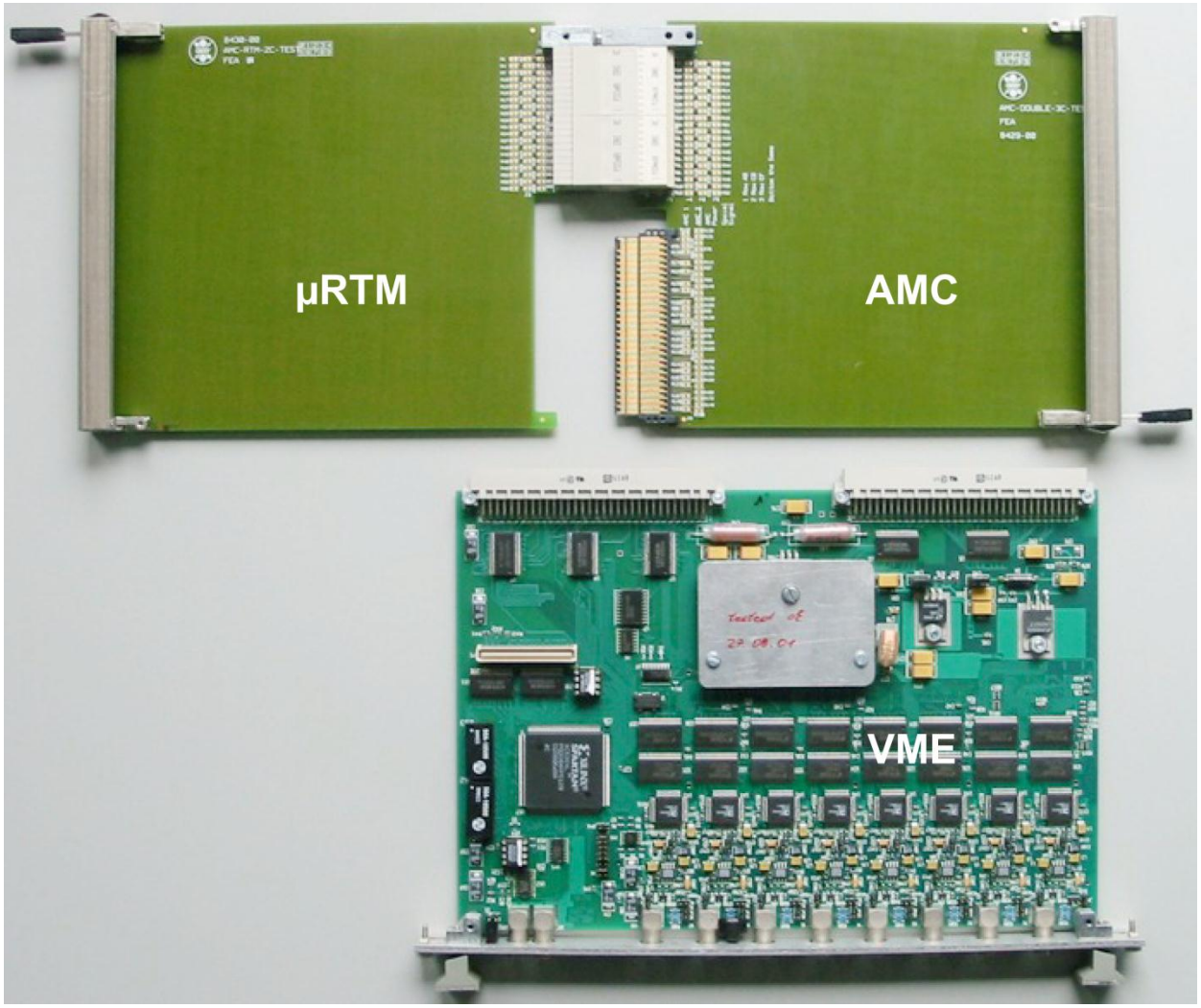
Pairs → Row# ↓	Gnd	F	E	Gnd	D	C	Gnd	B	A
1	GND[9]	P2[9]-	P2[9]+	GND[9]	P1[9]-	P1[9]+	GND[9]	P0[9]-	P0[9]+
2	GND[8]	P2[8]-	P2[8]+	GND[8]	P1[8]-	P1[8]+	GND[8]	P0[8]-	P0[8]+
3	GND[7]	P2[7]-	P2[7]+	GND[7]	P1[7]-	P1[7]+	GND[7]	P0[7]-	P0[7]+
4	GND[6]	P2[6]-	P2[6]+	GND[6]	P1[6]-	P1[6]+	GND[6]	P0[6]-	P0[6]+
5	GND[5]	P2[5]-	P2[5]+	GND[5]	P1[5]-	P1[5]+	GND[5]	P0[5]-	P0[5]+
6	GND[4]	P2[4]-	P2[4]+	GND[4]	P1[4]-	P1[4]+	GND[4]	P0[4]-	P0[4]+
7	GND[3]	P2[3]-	P2[3]+	GND[3]	P1[3]-	P1[3]+	GND[3]	P0[3]-	P0[3]+
8	GND[2]	P2[2]-	P2[2]+	GND[2]	P1[2]-	P1[2]+	GND[2]	P0[2]-	P0[2]+
9	GND[1]	P2[1]-	P2[1]+	GND[1]	P1[1]-	P1[1]+	GND[1]	P0[1]-	P0[1]+
10	GND[0]	P2[0]-	P2[0]+	GND[0]	P1[0]-	P1[0]+	GND[0]	P0[0]-	P0[0]+

µRTM User I/O, Management (J30)

Pairs → Row# ↓	Gnd	F	E	Gnd	D	C	Gnd	B	A
1	GND[9]	TDO	TCK	GND[9]	SDA	PS#	GND[9]	PWR	PWR
2	GND[8]	TMS	TDI	GND[8]	SCL	MP	GND[8]	PWR	PWR
3	GND[7]	P2[7]-	P2[7]+	GND[7]	P1[7]-	P1[7]+	GND[7]	P0[7]-	P0[7]+
4	GND[6]	P2[6]-	P2[6]+	GND[6]	P1[6]-	P1[6]+	GND[6]	P0[6]-	P0[6]+
5	GND[5]	P2[5]-	P2[5]+	GND[5]	P1[5]-	P1[5]+	GND[5]	P0[5]-	P0[5]+
6	GND[4]	P2[4]-	P2[4]+	GND[4]	P1[4]-	P1[4]+	GND[4]	P0[4]-	P0[4]+
7	GND[3]	P2[3]-	P2[3]+	GND[3]	P1[3]-	P1[3]+	GND[3]	P0[3]-	P0[3]+
8	GND[2]	P2[2]-	P2[2]+	GND[2]	P1[2]-	P1[2]+	GND[2]	P0[2]-	P0[2]+
9	GND[1]	P2[1]-	P2[1]+	GND[1]	P1[1]-	P1[1]+	GND[1]	P0[1]-	P0[1]+
10	GND[0]	P2[0]-	P2[0]+	GND[0]	P1[0]-	P1[0]+	GND[0]	P0[0]-	P0[0]+

No ENABLE# signal

Board size comparison – VME/double-size µTCA

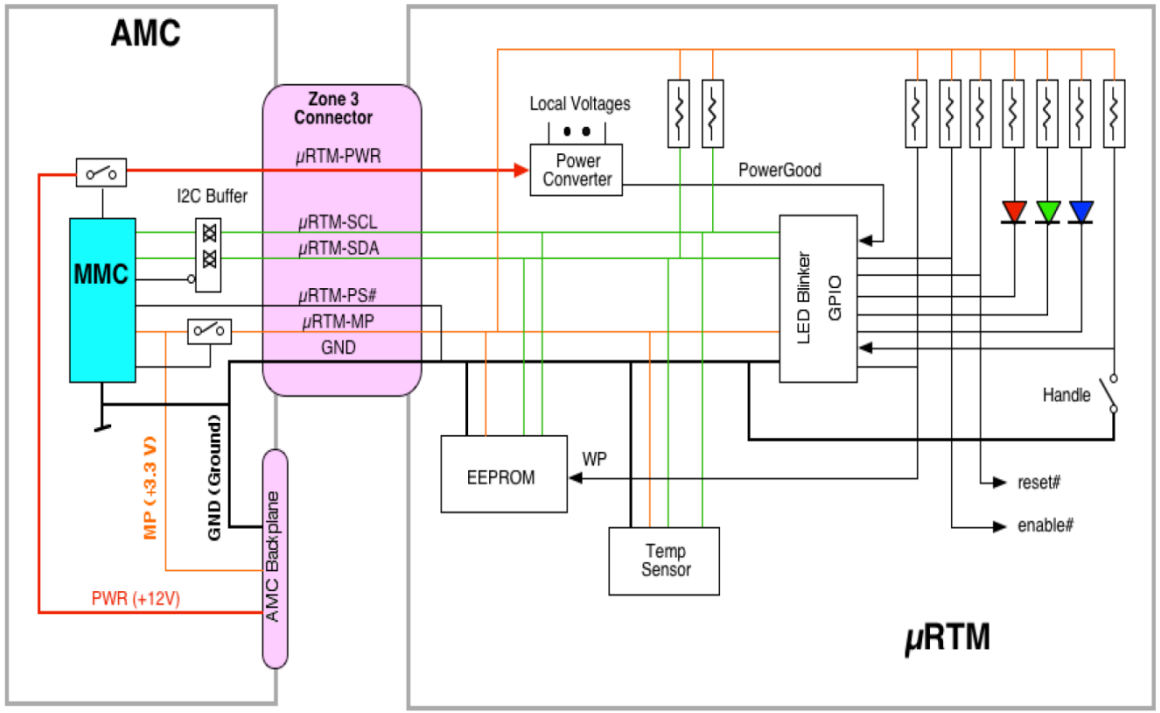


AMC + RTM:
~457 cm^2

VME:
~345 cm^2

MTCA.4 Management

The AMC/µRTM pair are viewed as one unit from the system



- Safety mechanical key implemented
- Short pin to indicate full insertion or removal
- µRTM has a serial PROM that communicates with the front AMC module's MMC
- Data read from the PROM is used by the system manager for enabling the µRTM 12v converter
- LED's, handle switch, etc are controlled and/or read through I2C

EEPROM: FRU Data

length	field
1	Common header
1	Internal
1	Chassis info area = 0
1	Board area
1	Product area
1	Multi record area
1	PAD = 0
1	Checksum

length	Board, Product field
3	Header, length, language
3	Mfg. Date / time
1 + P	Board manufacturer
1 + Q	Board product name
1 + N	Board serial number
1 + R	FRU file ID, version
xx	Additional custom info
1 + Y	End mark, unused space
1	checksum

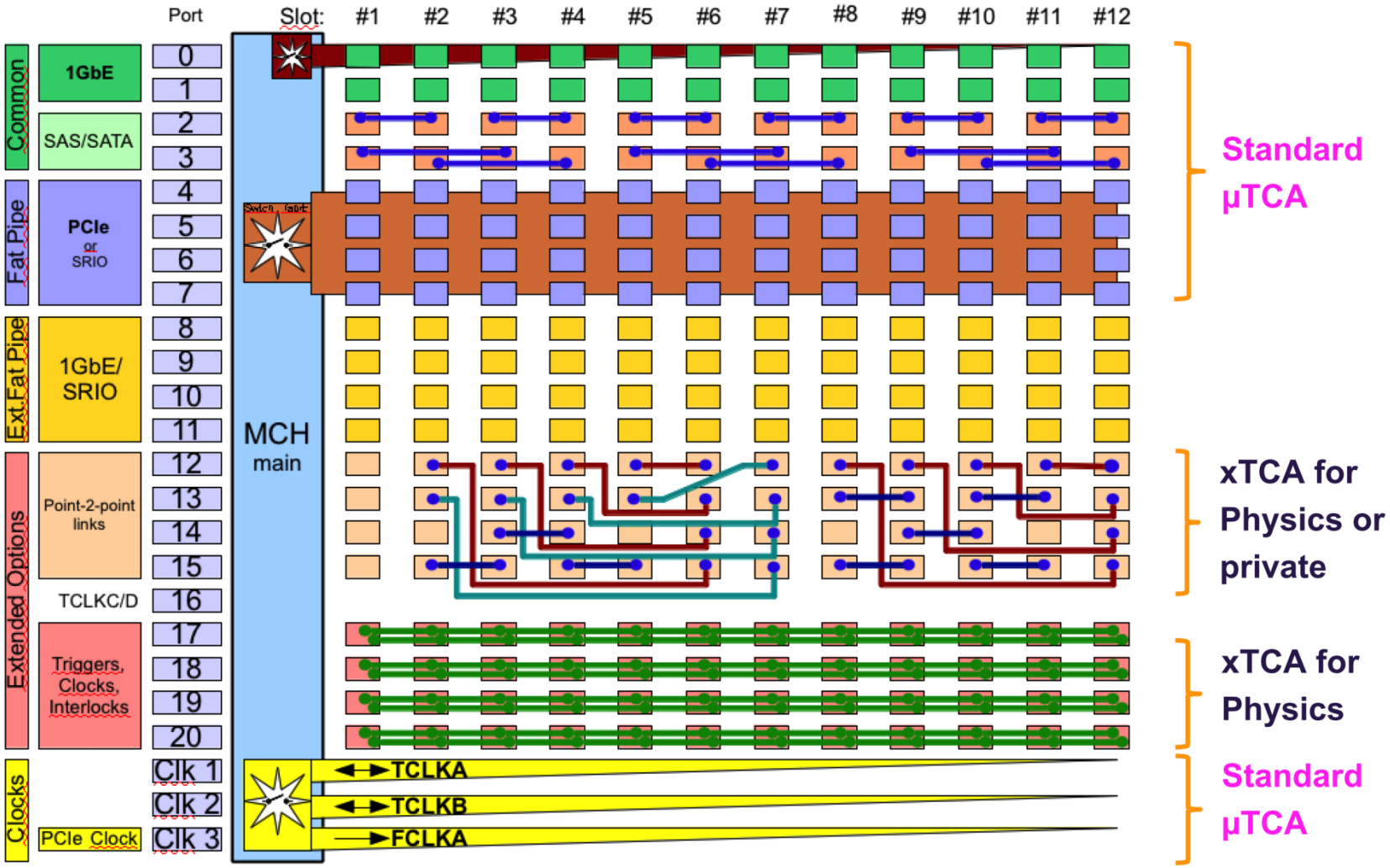
length	SDR record field
5	Sensor record header (type..)
3	Record key bytes (owner)
N	Record body bytes
	Next sensor record……

Multi records
Power/current consumption header
Power/current consumption data
Link info header
Link info data
Termination header

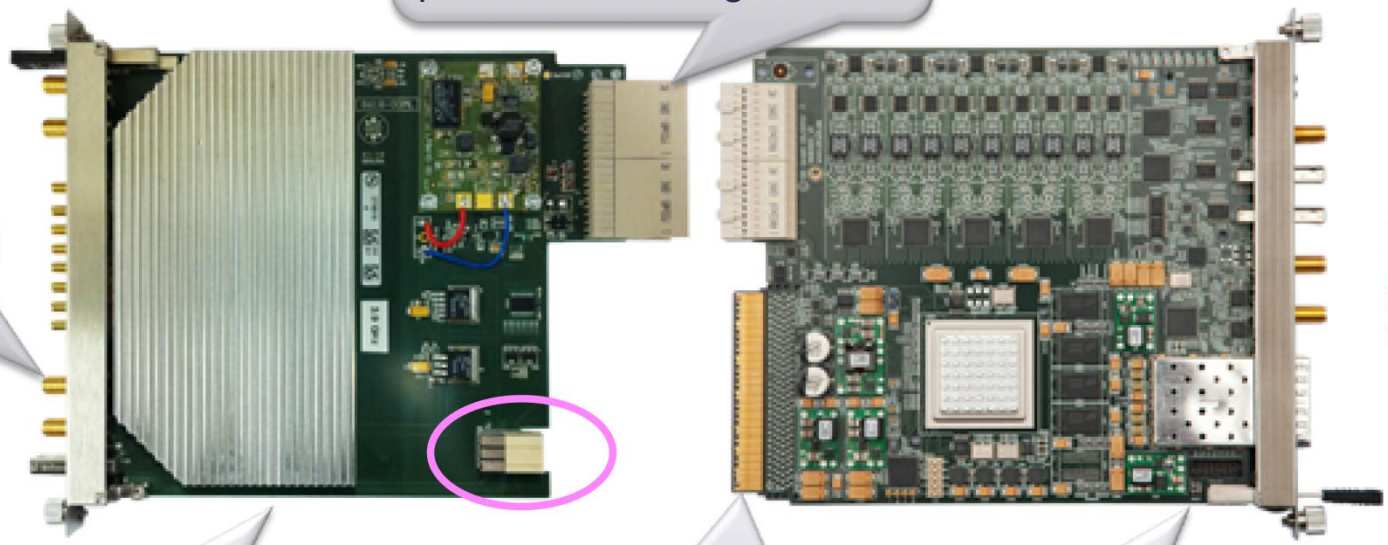
MTCA.4 Physics Backplane

- The MTCA.4 backplane specifies module interconnect features required for many Physics research environments:
  - Clock distribution
  - Interlocks
  - Analog summing of signals or other, user defined
- It uses the Extended Options region for Physics features
- Any AMC module that does not use this region will work when inserted on the redefined backplane
- The backplane is not used by the µRTM

MTCA.4 Backplane



MTCA.4 double size AMC and µRTM (implementation)



Connector:
Analog or digital signals, power and management

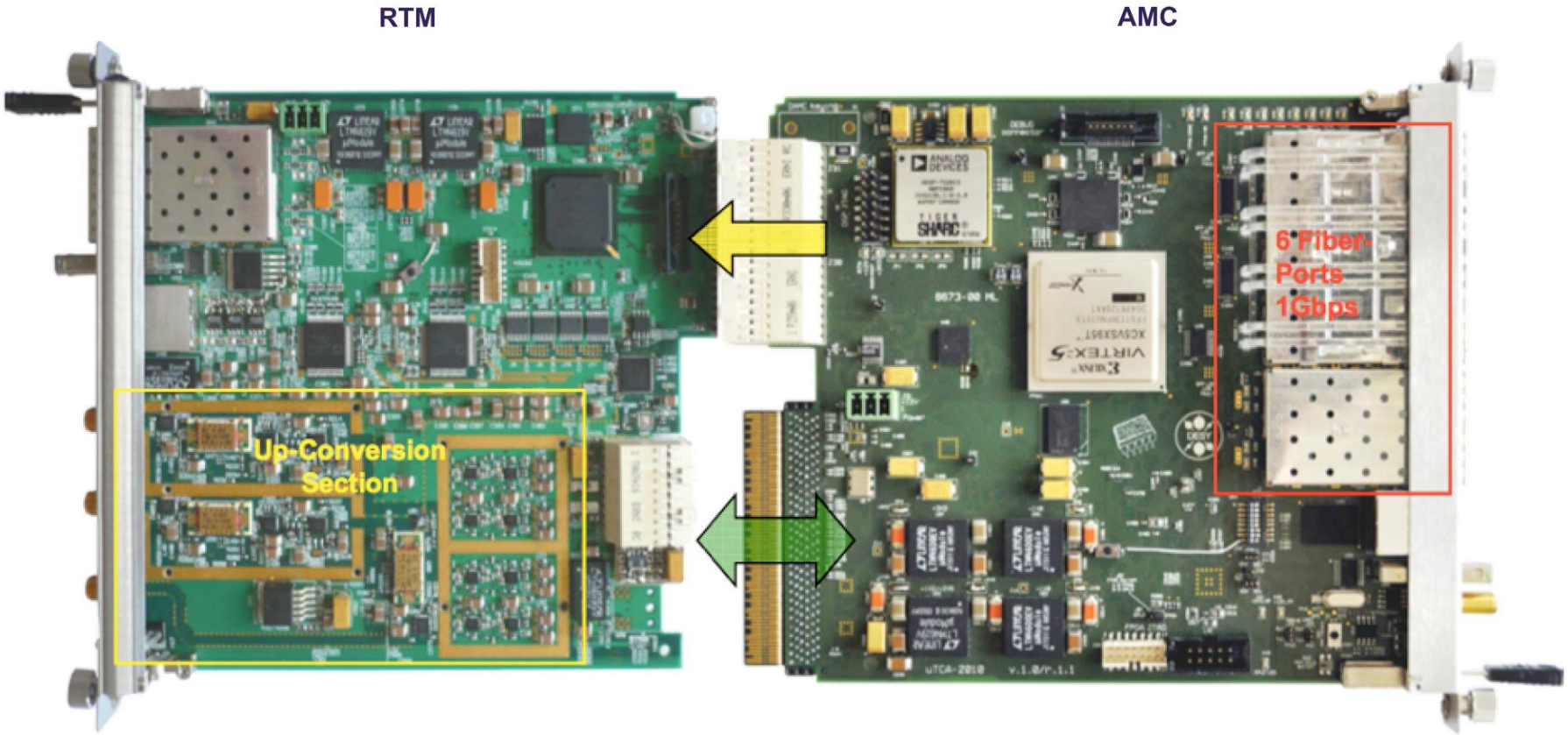
Cables from rear
e.g. SMA 1.3GHz

µRTM:
I/O adapter,
Application specific signal conditioning and cable adapters

AMC connector:
Ethernet and PCIe, Clock and Trigger

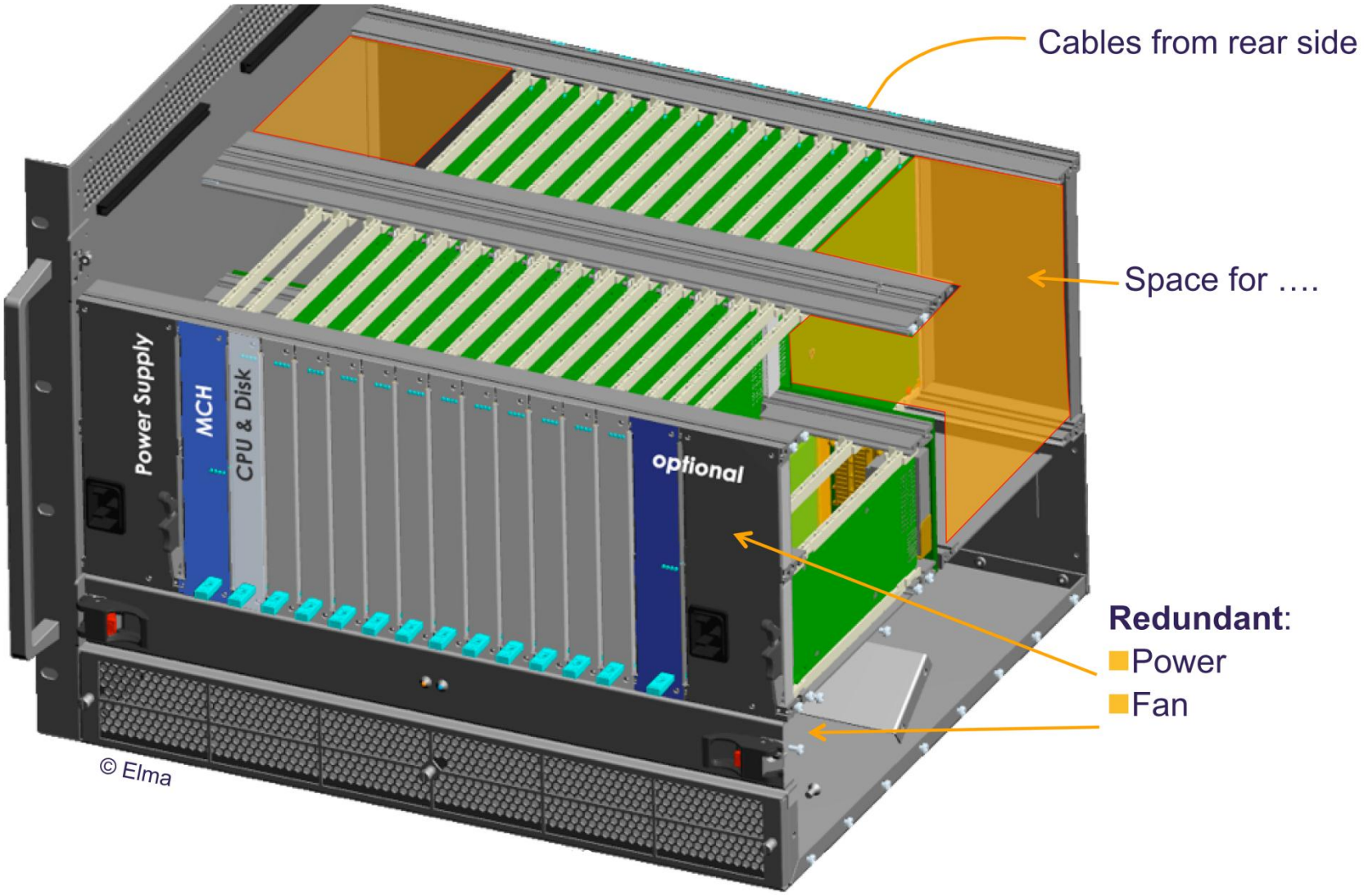
Standard front **AMC**:
FPGA with high speed data links,

Digital AMC and Analog µRTM



- 2 ch Vector Modulator:
  - 1.3 GHz … 3.9 GHz
  - 16 bit DAC
- LLRF Controller:
  - 6 Fiber-Ports on front
  - 8 Gb-Links to backplane

MTCA.4 Modular Unit



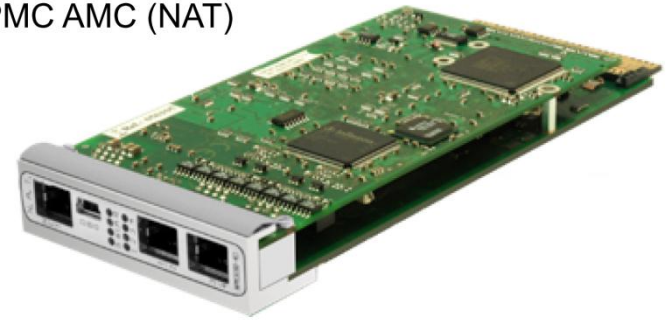
Examples of Commercial I/O AMCs

- IP Module carrier:
  - TAMC100/200 (Tews)

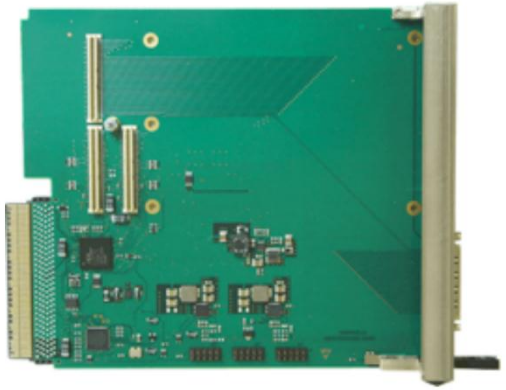
  - AMC703 (Hytec)

- ADIO24 Analog/digital IO (ESD)

- PMC Module carrier:
  - PMC AMC (NAT)



  - TAMC260 (Tews)



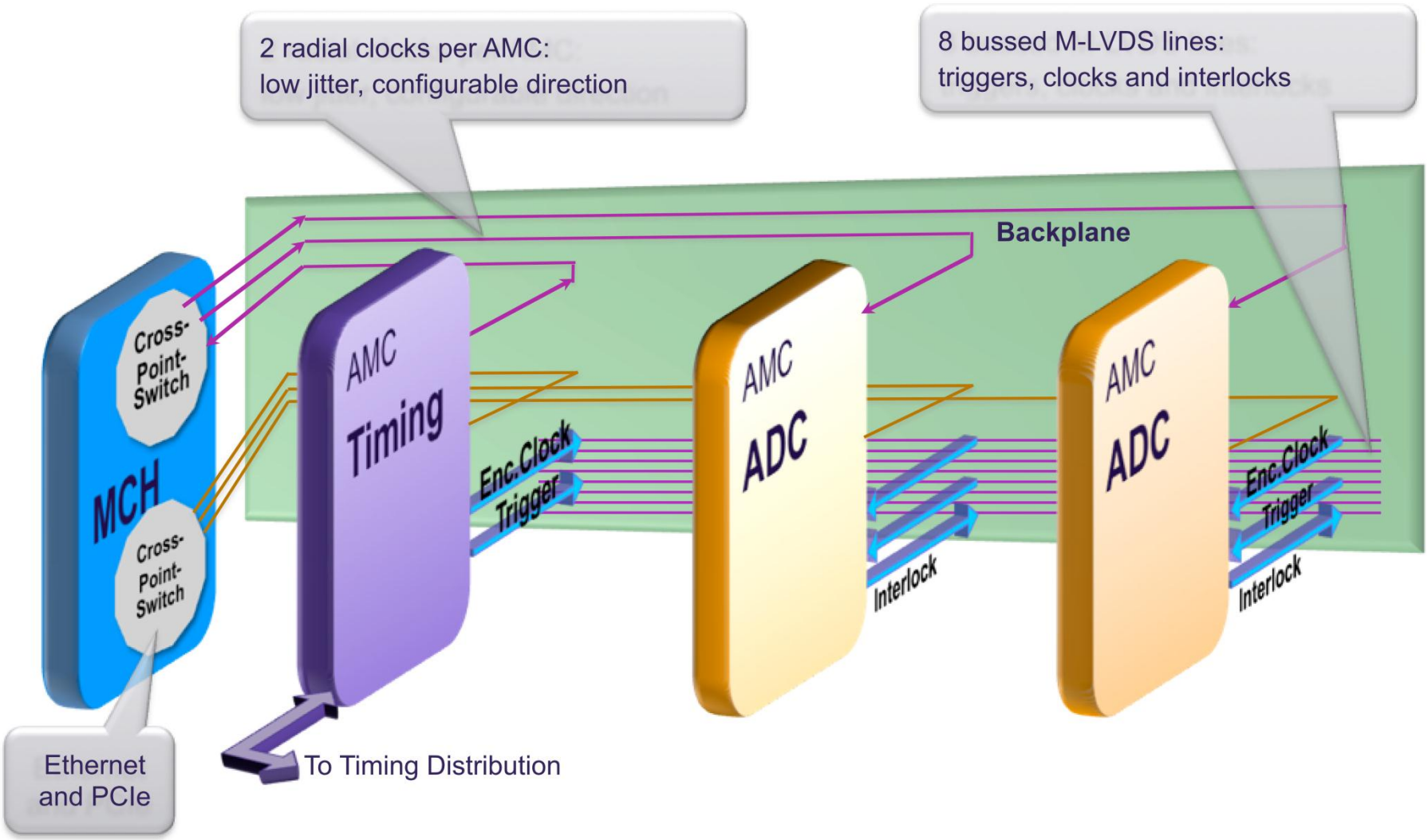
- FMC Module carrier:
  - TAMC631/640/641

D. Timing Extensions for AMC/µTCA

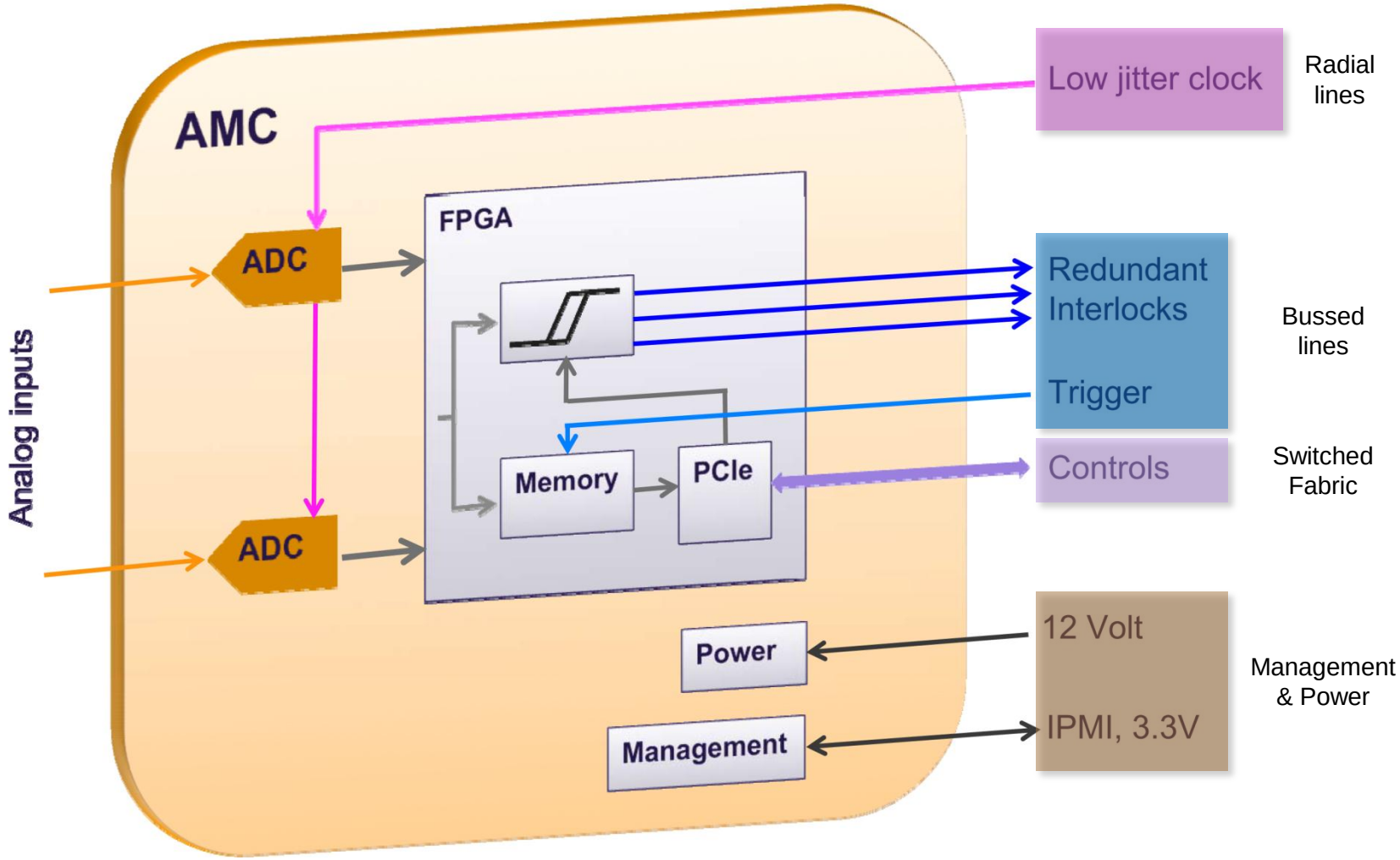
D. µTCA Precision Timing & Trigger Distribution Extensions

- The 12-slot µTCA shelf specified for Physics use includes the capability for distribution of precise timing and triggering
  - Existing 6-slot shelves do not provide redundant features but will include support of the timing features.
  - These features will require MCH's that can manage either 6 or 12 slots or both.
- Extended Options radial lines are used, managed by the MCH
  - To provide point-to-point buffered lines for good isolation between modules, thus:
  - allowing removing a module in a hot-swap operation without perturb timing signals in adjacent modules.
- A new concept defines that a timing source in any slot may drive any other applications slot.
- Additional lines were added to the new backplane layer
  - For the non-precise bus lines.
  - For special summing and daisy-chain lines for vector summing involving several modules and slow interlocks involving several modules.

uTCA: Clocks, Triggers and Interlocks

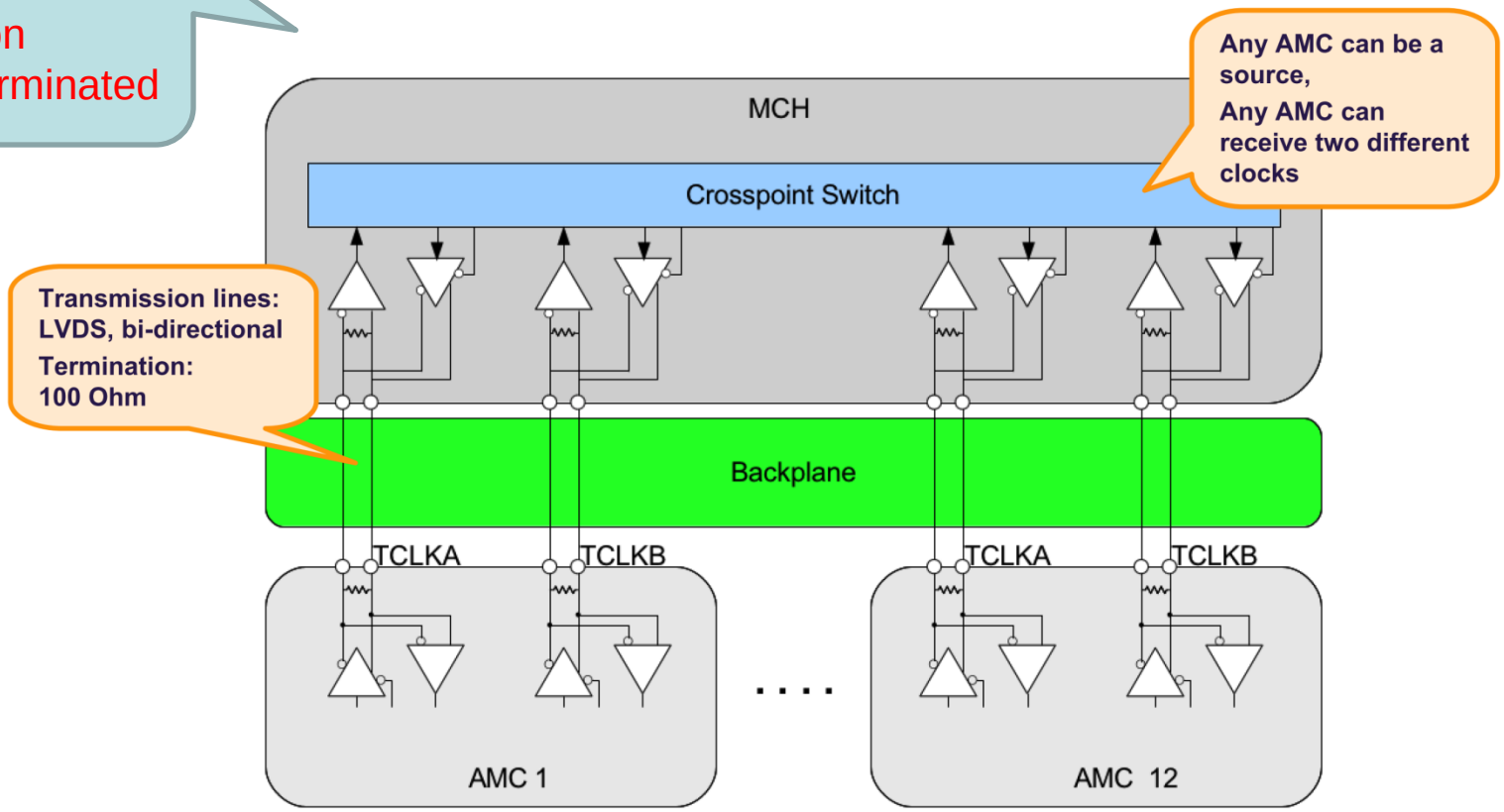


I/O Module Example

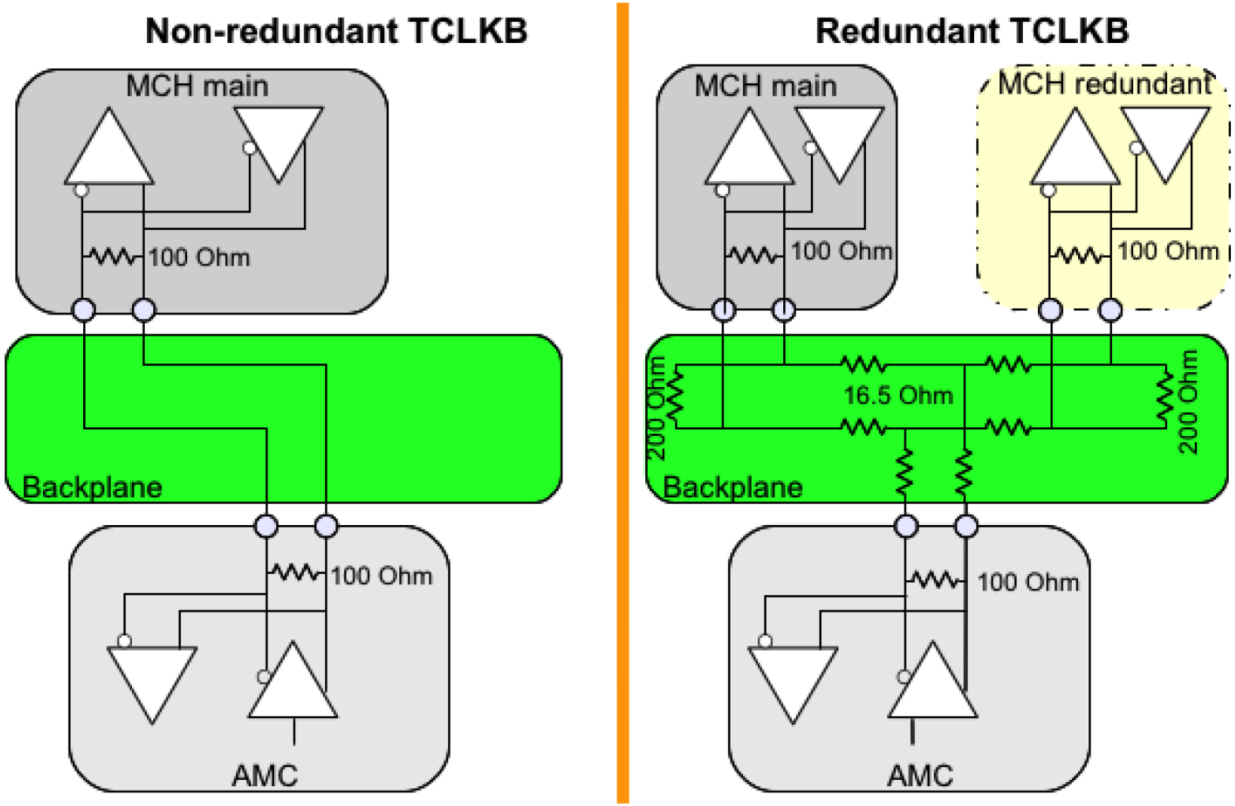


Radial Low Jitter Clocks

- Point-to-point
- High precision
- Both ends terminated

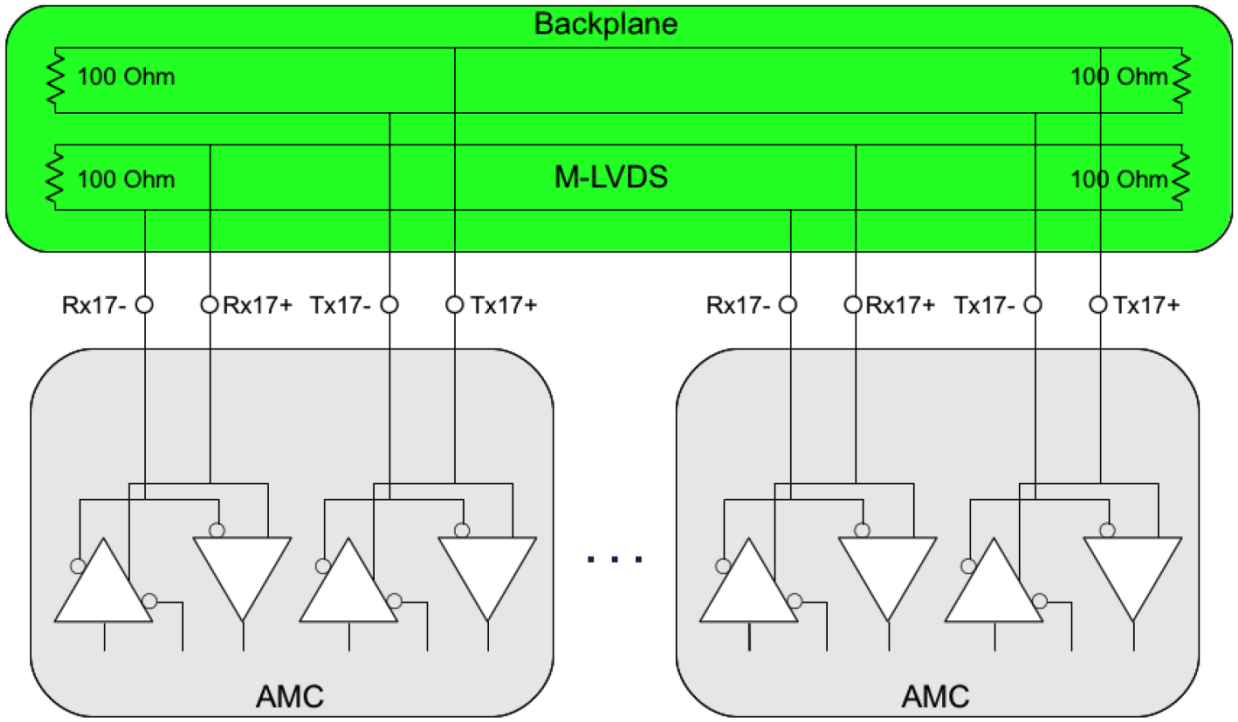


Optional Redundant Radial Clock



Bused Lines for Trigger, Gate, Clock and Interlock

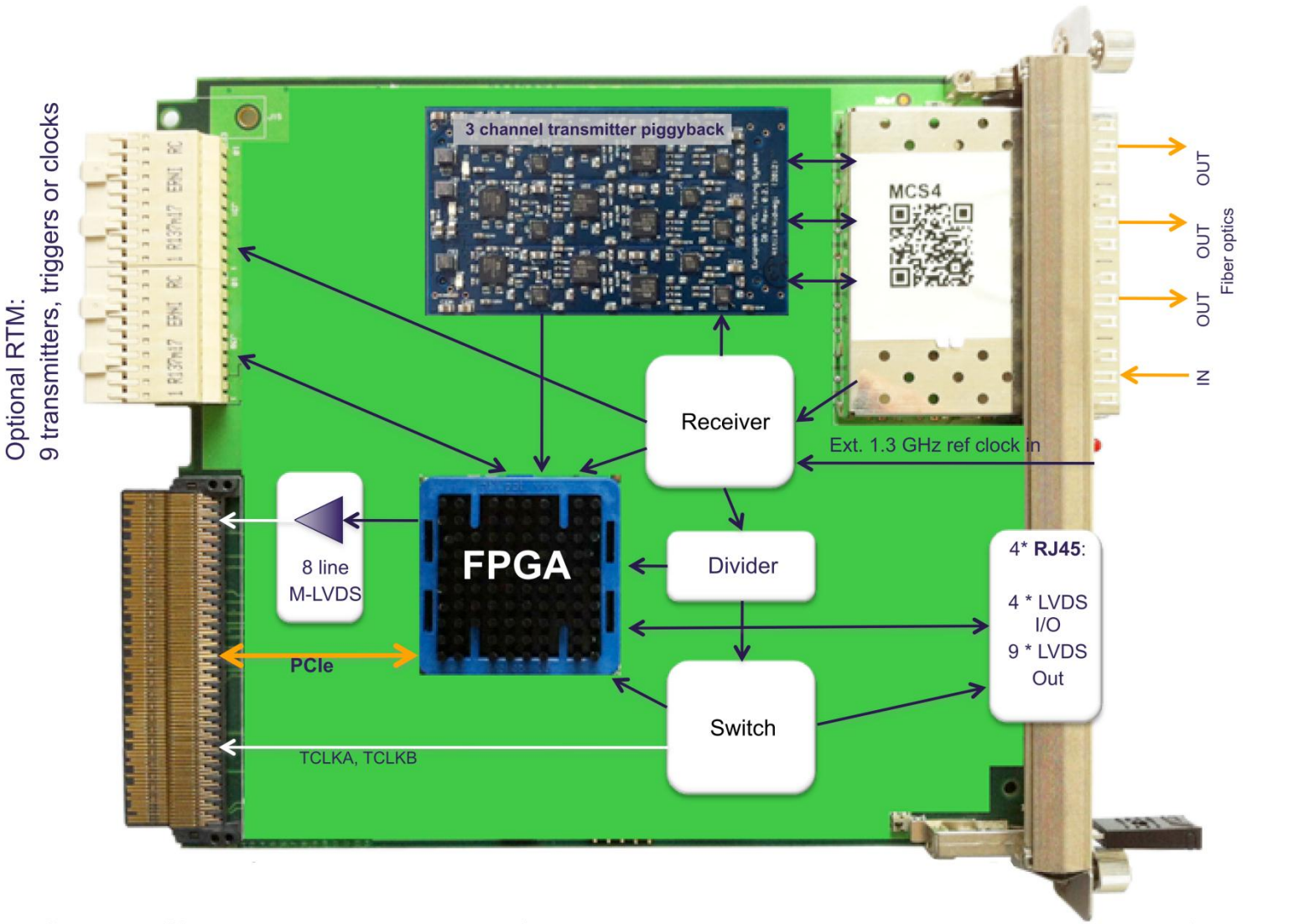
- **Multi-Point LVDS**, 8 lines
- Can be used for:
  - Clocks
  - Triggers
  - Gates
  - Time-stamp
  - Data transfer (FPGA-2-FPGA)
- All AMCs can be
  - Receiver, Transmitter, or disabled



AMC.0 / µTCA port compatibility

Connector Region		AMC Port #	Signal Convention			Non-redundant MCH Fabric #	Redundant MCH Fabric #
Basic Side	Common Options	0	AMC.2 1000BASE-BX			A	1 / A
		1	AMC.2 1000BASE-BX				2 / A
		2	AMC.3 SATA/SAS			(B)	(1 / B)
		3	AMC.3 SATA/SAS			(C)	(2 / B)
	Fat Pipe	4	AMC.1 X4 PCIe	AMC.4 X4 SRIO	AMC.2 10GBase-BX4	D	1 / D
		5				E	1 / E
		6				F	1 / F
		7				G	1 / G
Extended Side	Extended Fat Pipe	8	AMC.1 X8 PCIe	AMC.4 X4 SRIO	AMC.2 10GBase-BX4		2 / D
		9					2 / E
		10					2 / F
		11					2 / G
	Extended Options	12	MTCA.4 X4 application specific wire-ring	*Not specified*			
		13					
		14					
		15					
		16					
		17	MTCA.4 X4 M-LVDS timing bus	AMC.4 X4 SRIO			
		18					
		19					
		20					

MTCA.4 Timing Implementation Example (XFEL)



E. Software Guidelines Development

E. Software Guidelines Development

- Purpose is:
  - To facilitate availability of COTS solutions
  - To facilitate and inter-operability/re-usability between facilities and projects

  by defining common techniques and modules for software development
- General topics
  1. Routing and Protocols
  2. System/Rack/Module Management
  3. Operating Systems and Infrastructure
  4. Processing and Operations Libraries
- Primary focus: In-rack and embedded components
- Approach: Identify, integrate, and provide examples for existing industry standards
- Expected products
  - Guidelines (not “standards”) for development in the ATCA/µTCA instrumentation environment
  - Publicly-available reference implementations

1. Guidelines for: Routing and Protocols

- Data Protocols
  - Via ATCA/µTCA fabric interface
  - Common channel types/configurations
    - “Low” Latency (< ~100ns)
    - “Medium” Latency (< ~1µs)
    - “High” Latency (> ~1µs)
    - Examples: Custom binary point-to-point, PCIe, SRIO, Ethernet (1G/10G/40G)
  - Software Support: Standardized connection and traffic management
- Timing/Synchronization Protocols
  - Via ATCA/µTCA clock and/or fabric channels
  - Standard synchronization elements
    - Clocks
    - Triggers
    - Interlocks
  - Software Support: Standardized connection and configuration
- Command/Control
  - Application-oriented: augments system/rack/module management facilities
  - Primary: via ATCA/µTCA base interface (1G Ethernet)
  - Software Support: Standard channel-agnostic protocol

2. Guidelines for: System / Rack / Module Management

- Remote management functions
  - Rack/Module identification
  - Health/Status monitoring
  - Redundancy/Failover management
  - Resource management
  - In-field firmware/software update
- Rack/Module management
  - Utilizes standard IPMI/HPI protocols and channels from ATCA/µTCA and SAF
  - Primary effort is identifying and documenting how to use the IPMI/HPI facilities within the physics environment
  - A small number of extensions are required (example: incorporate analog signal formats into electronic keying)
- System Management (under consideration)
  - Common database for documenting external infrastructure (cable plant, actuators, sensors, etc.) utilized by Racks/Modules

IPMI: Intelligent Platform Management Interface
HPI: Hardware Platform Interface
SAF: Service Availability Forum

3. Guidelines for: Operating Systems & Infrastructure

- "Virtual Machine" environment for software development
  - Goal: operating-system independence at the application level
  - Goal: insulation from hardware details at the application level
  - Standardized components
    - Process/Thread management, scheduling, and communications
      - Examples: POSIX, EPICS
    - Hierarchical I/O, communication, and timing device structure and API
      - Supports local, remote, and "virtual" devices within the same framework
    - Hardware management API for custom board development

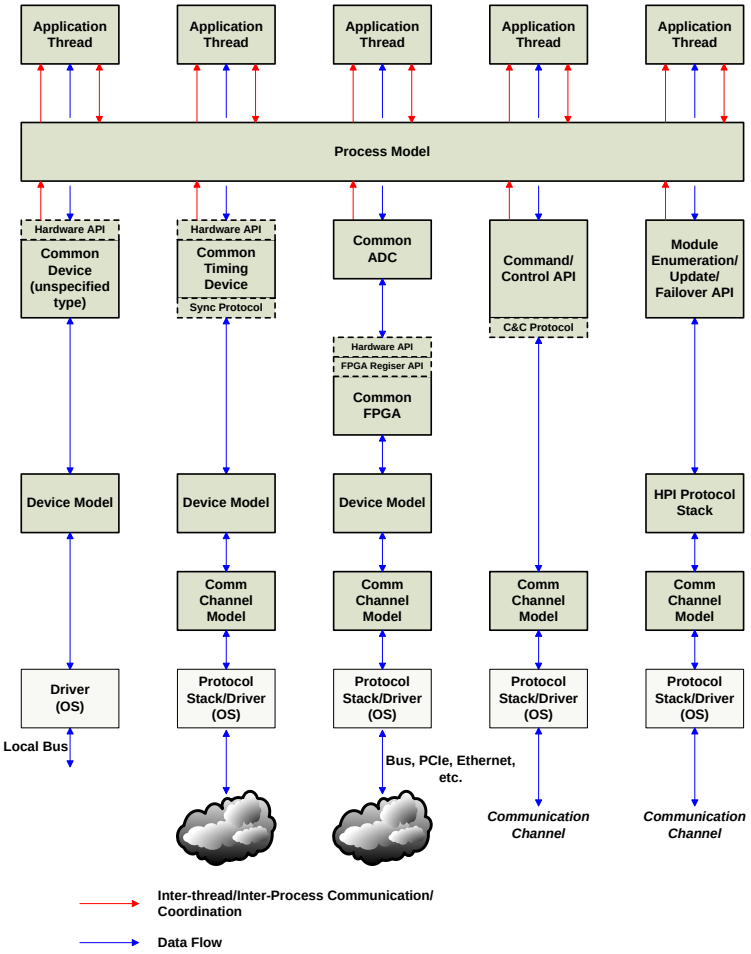
4. Guidelines for: Processing and Operation Libraries

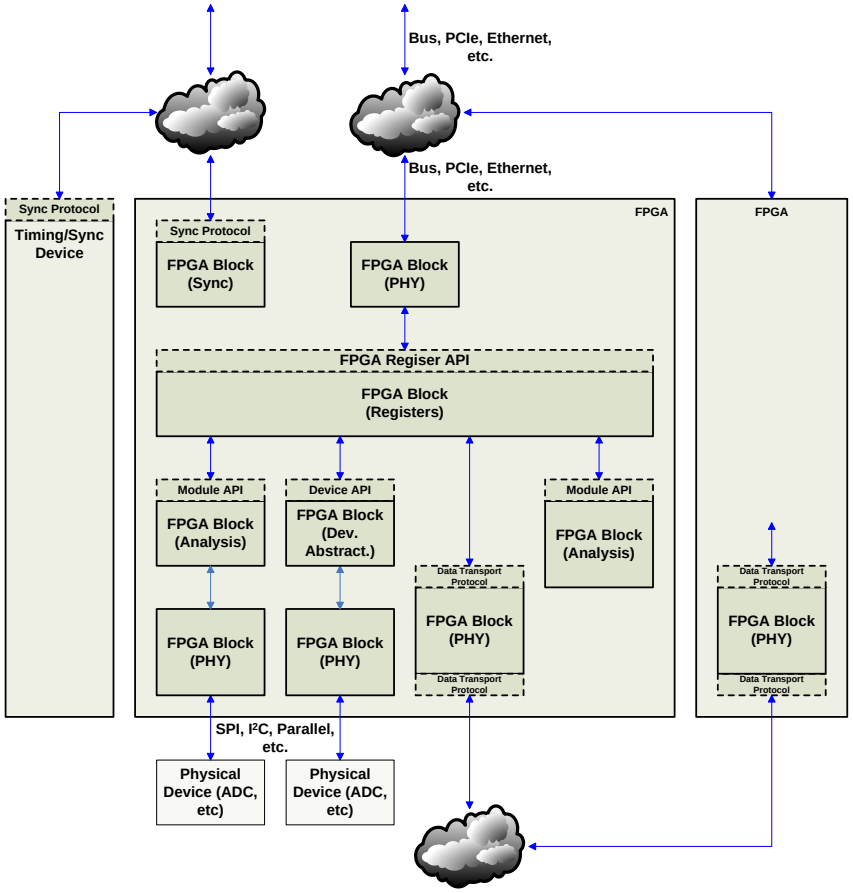
- Commonly-used components
  - Device-specific APIs (software)
    - Examples: ADC/DAC, timing/sync module, power supply controller, actuator controller, temperature sensor
  - Device-specific APIs (hardware registers)
  - Standard function libraries (software)
    - Examples: queue, math functions, signal filters, error handler, event logger, command/control parser
  - Standard function libraries (FPGA)
    - Examples: signal filters, high-resolution timer, low-latency communication channel, I^2C controller
- Reference Designs/Templates (software and FPGA)
  - Examples: thread-based control loop, signal processing chain, generalized signal acquisition/analysis system

Software Guidelines Development Working Groups

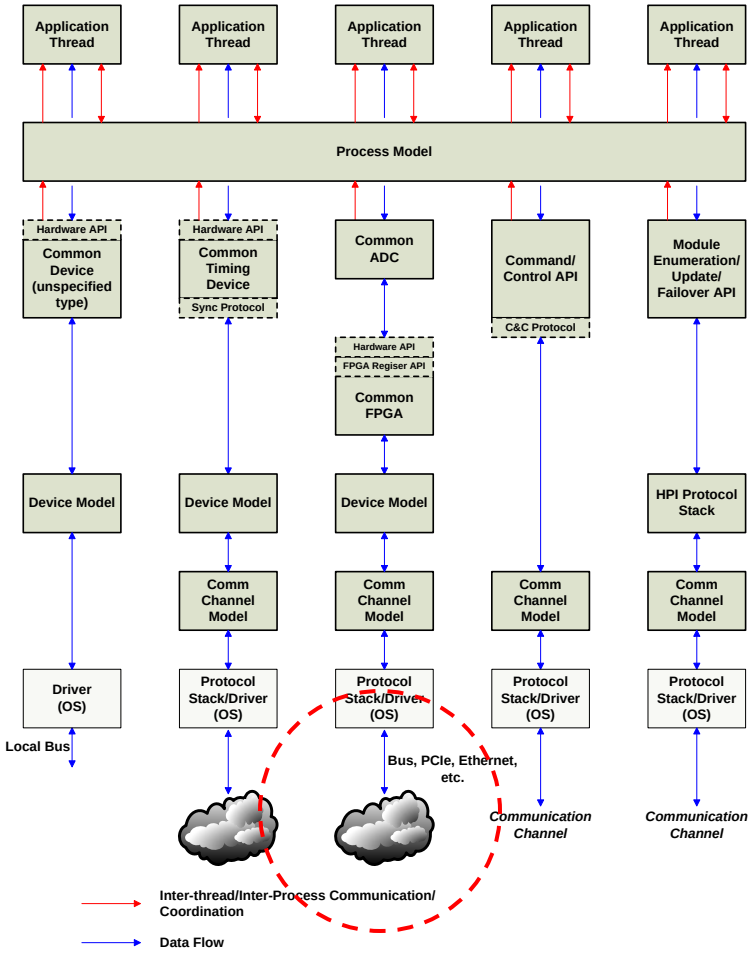
- Data Transport Protocol
  - Initial Protocol set selected and under evaluation
- Synchronization Protocol
  - Pending final hardware distribution scheme
- Command/Control Protocol
  - At discussion/proposal stage
- Component Management/Failover/Update
  - At discussion/proposal stage
- Standard Hardware API
  - Technical proposal accepted in principle; guideline in work
- Standard Process/Thread Model
  - Technical proposal accepted in principle; guideline in work
- Standard I/O Device Model
  - Technical proposal accepted in principle; guideline in work
- Standard Communication Model
  - Combined with Common I/O Device Model

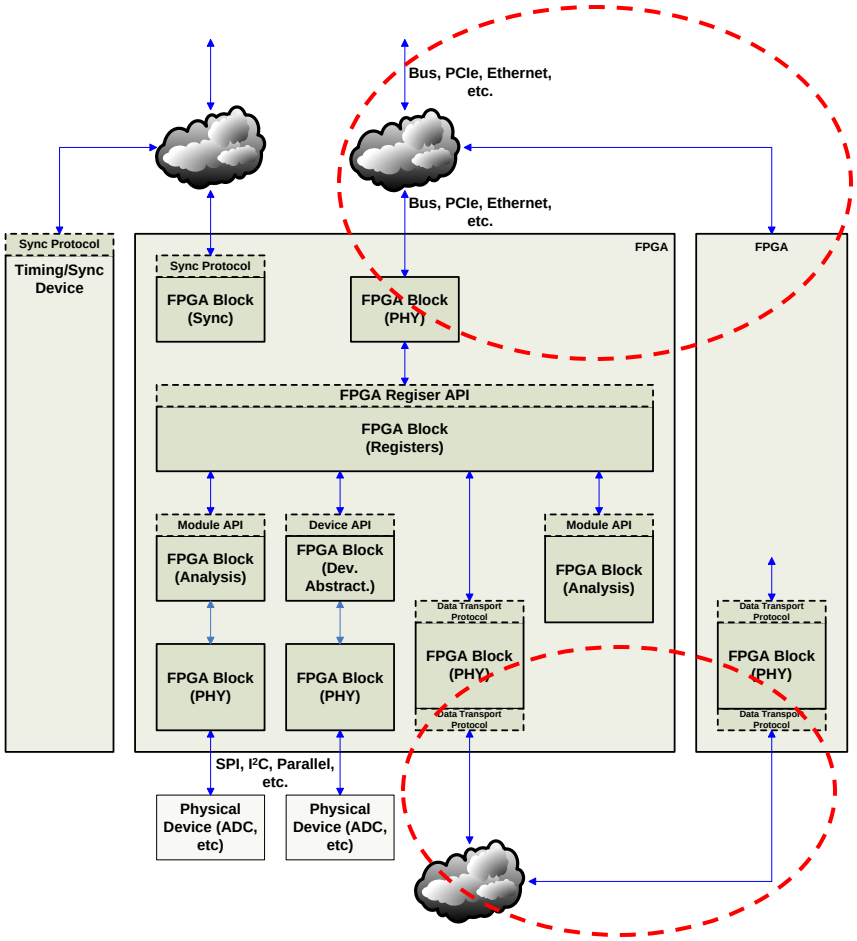
Software Application (example)



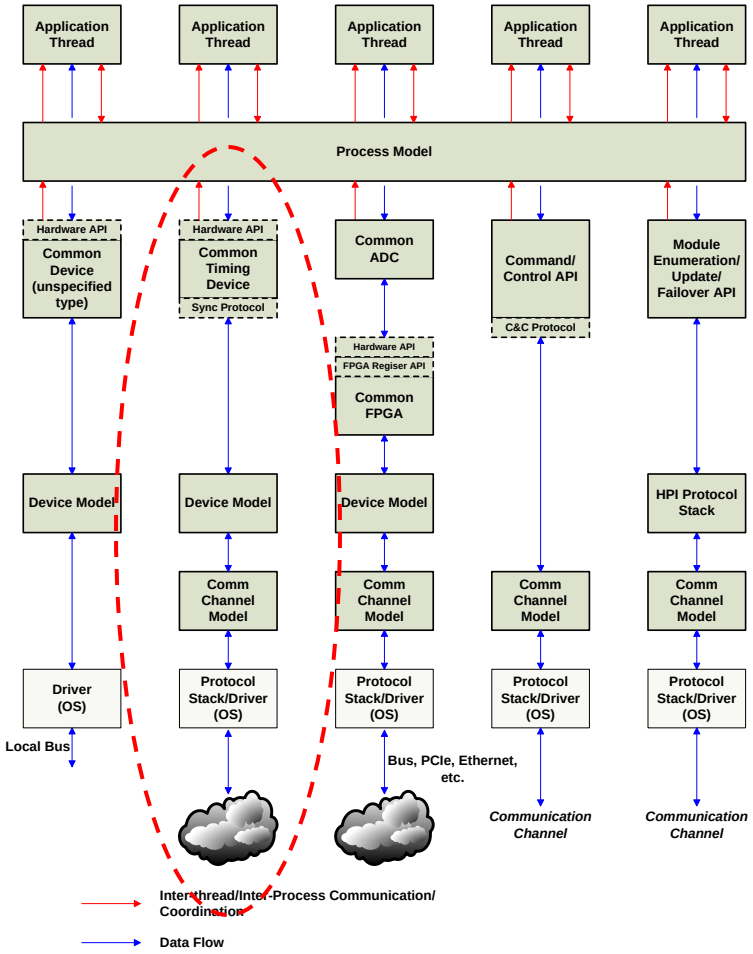


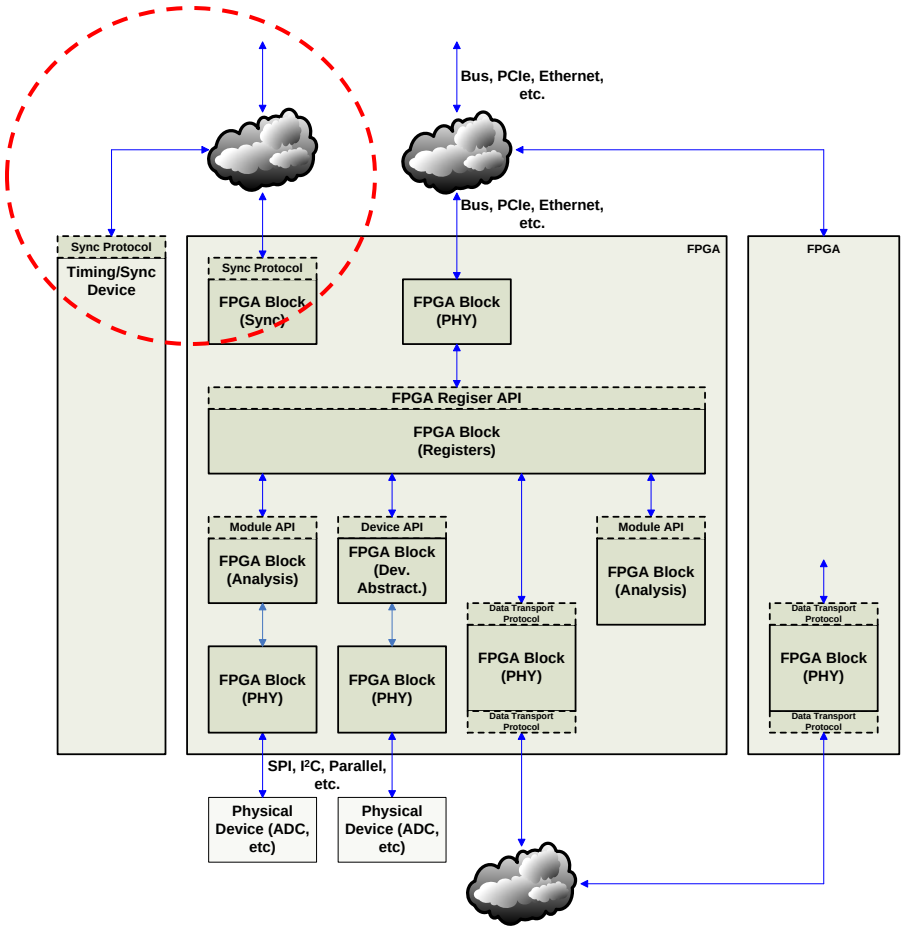
Data Transport Protocols



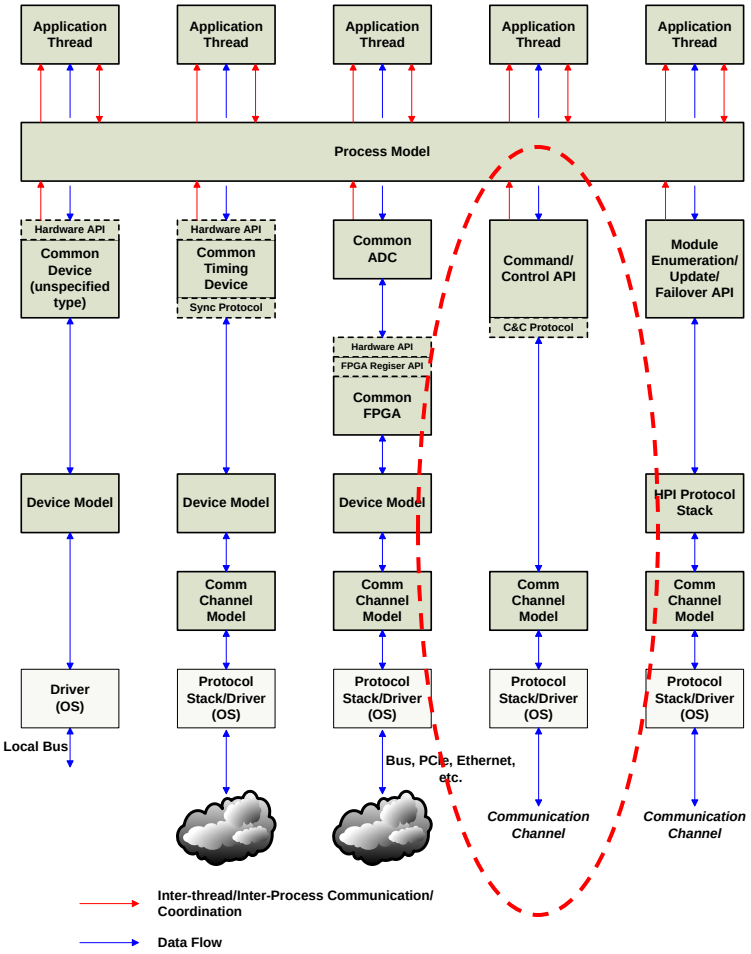


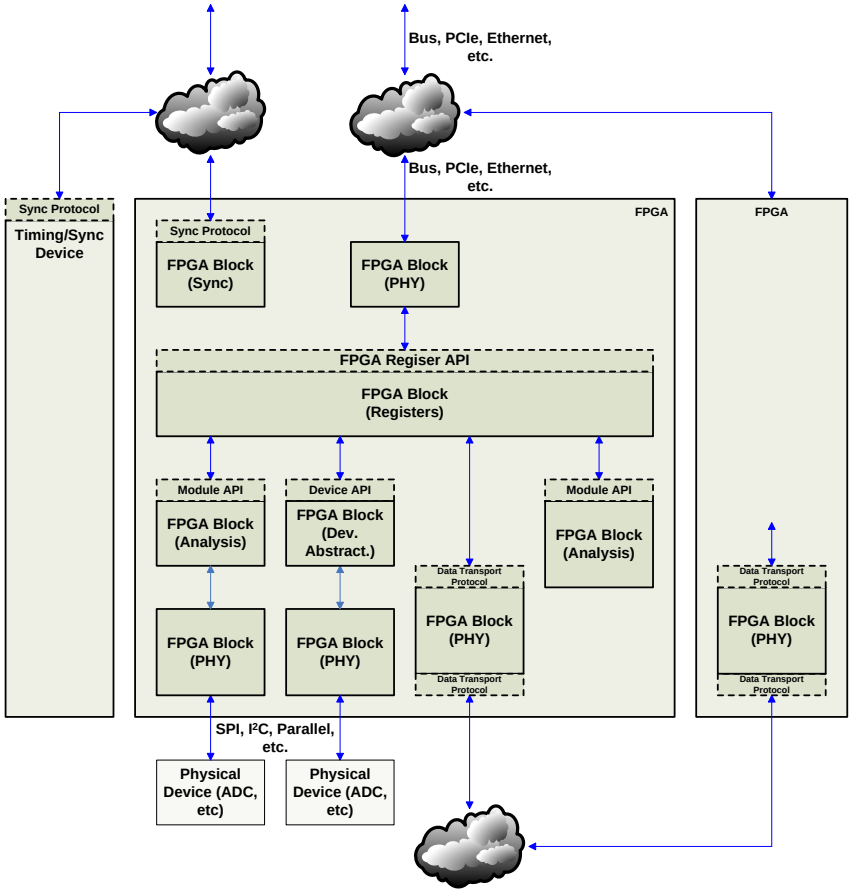
Synchronization Protocol



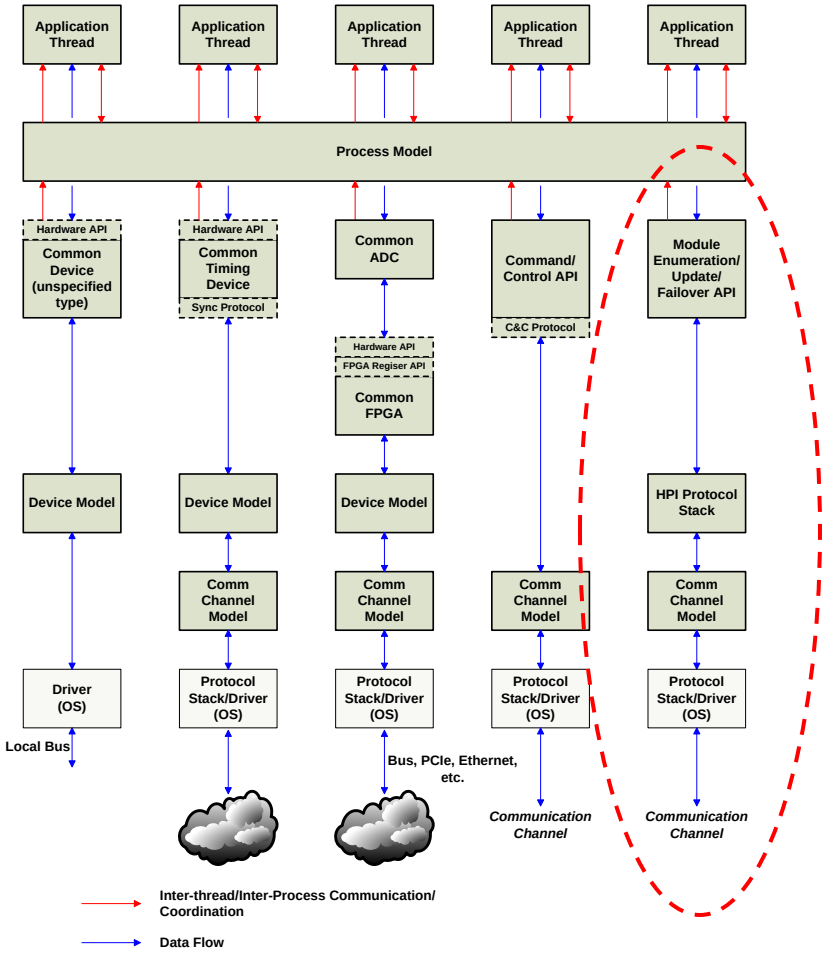


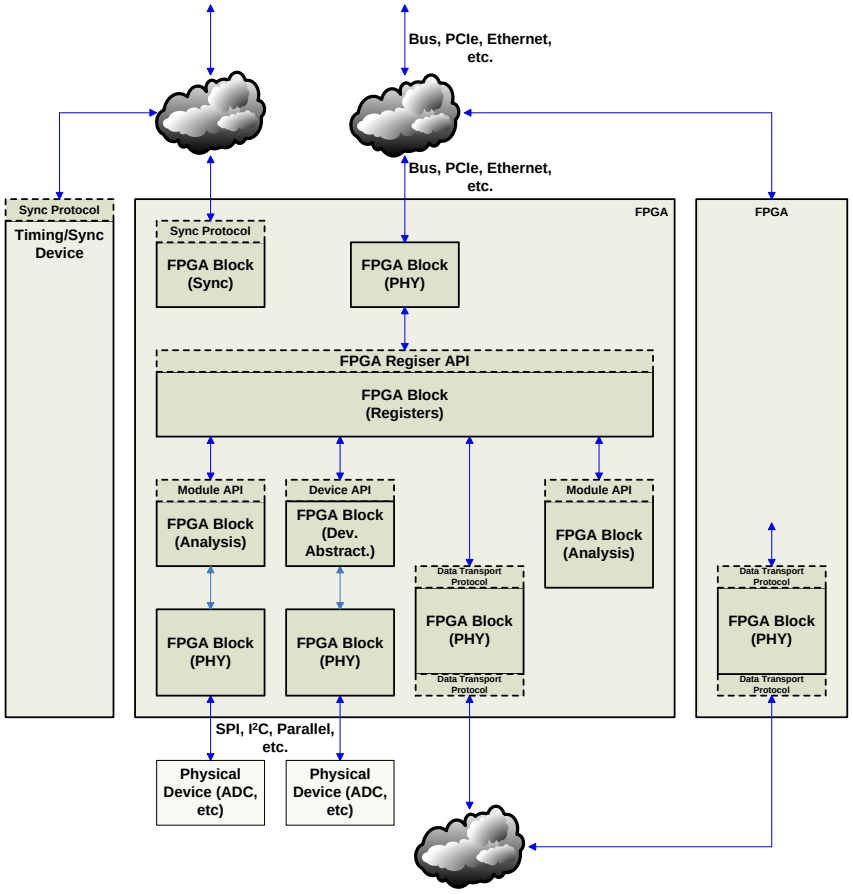
Command/Control Protocol



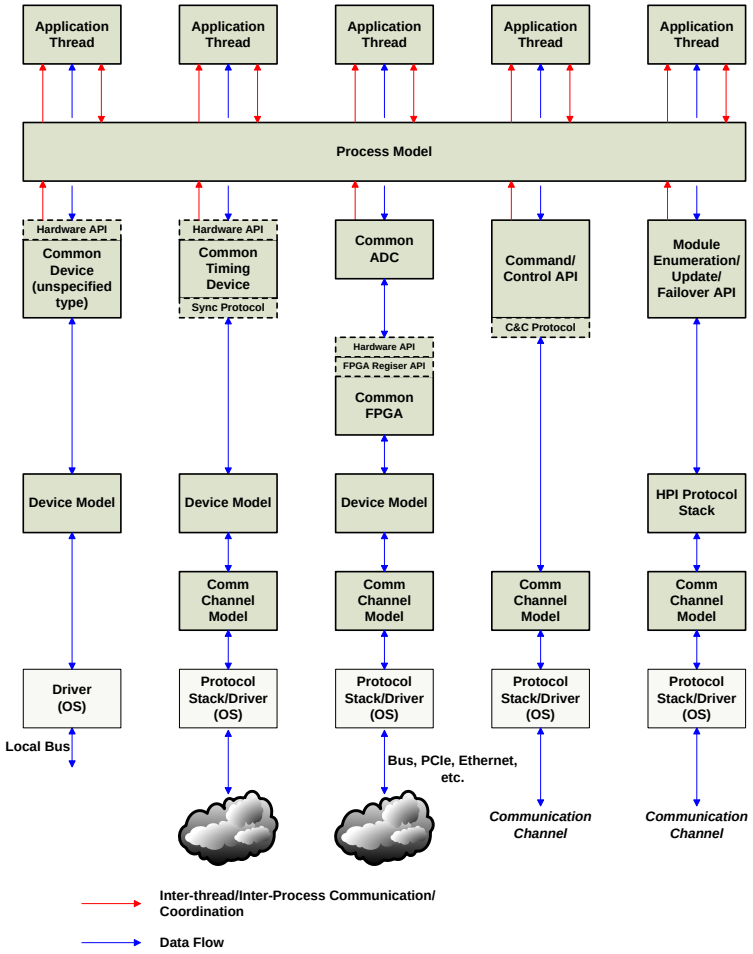


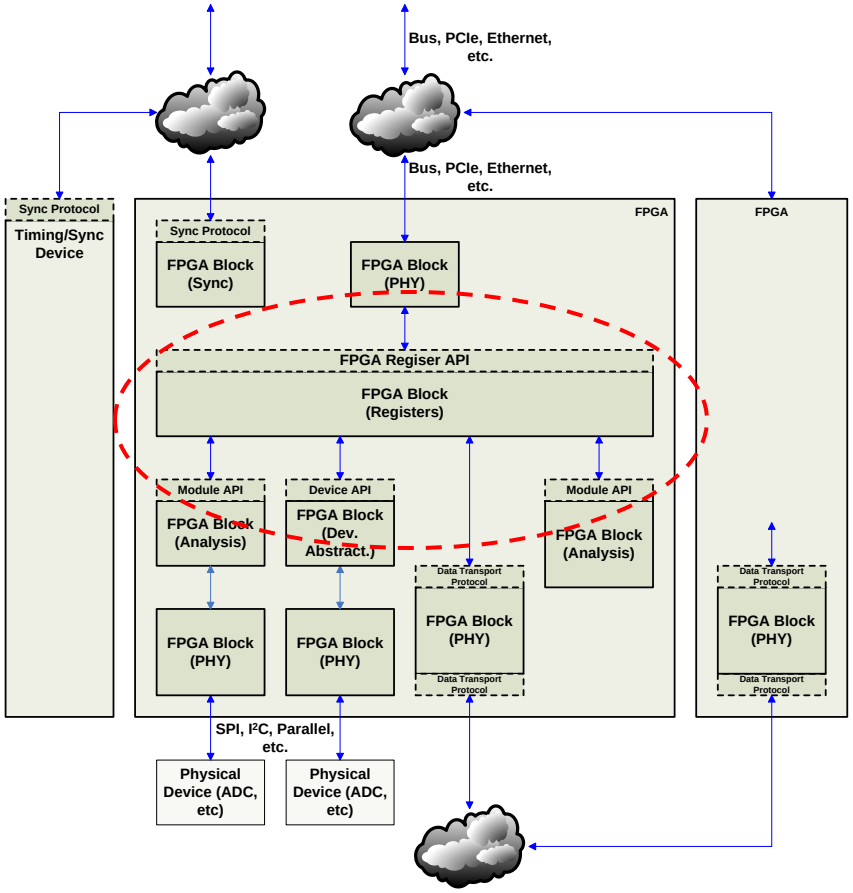
Component Management / Failover / Update



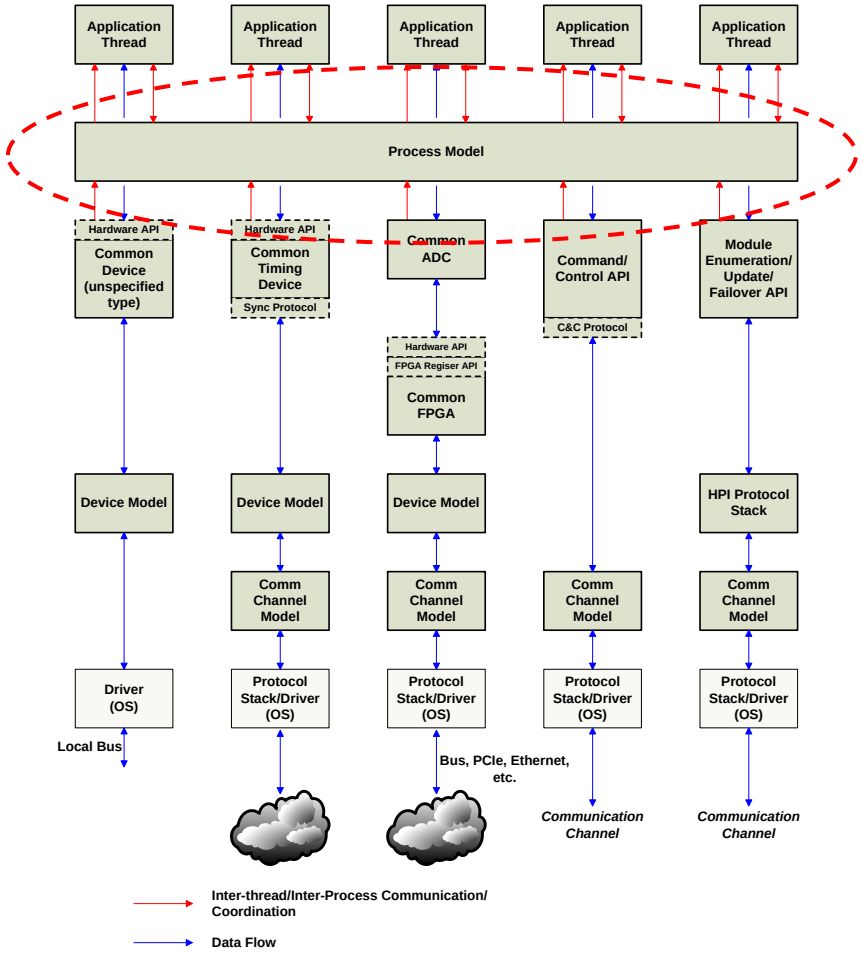


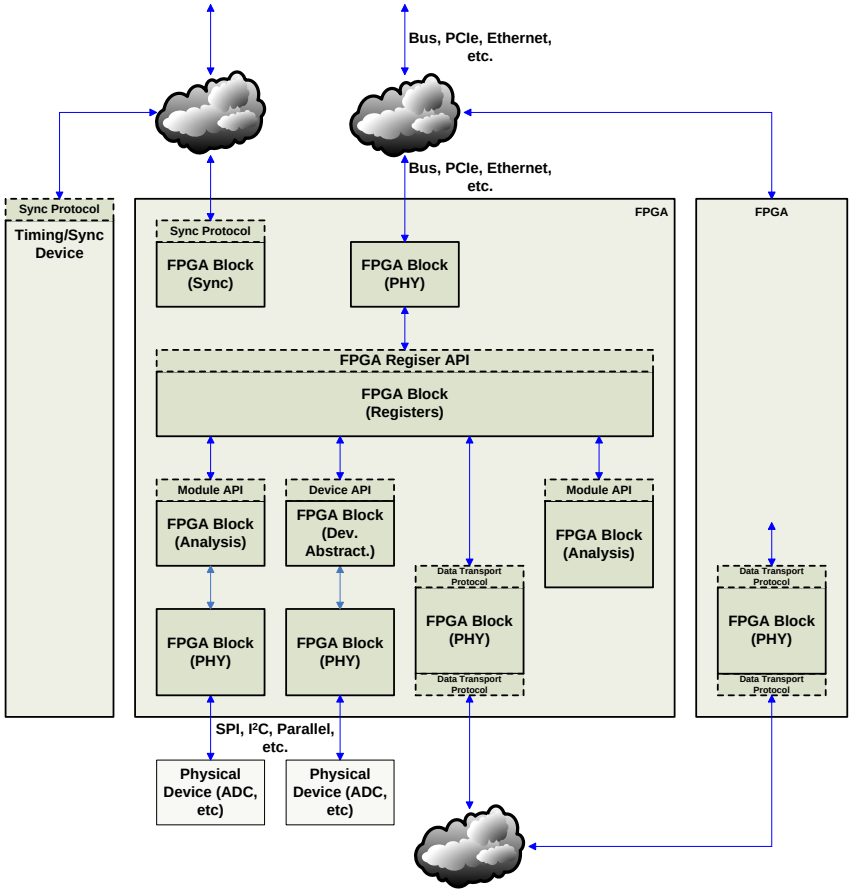
Standard Hardware API



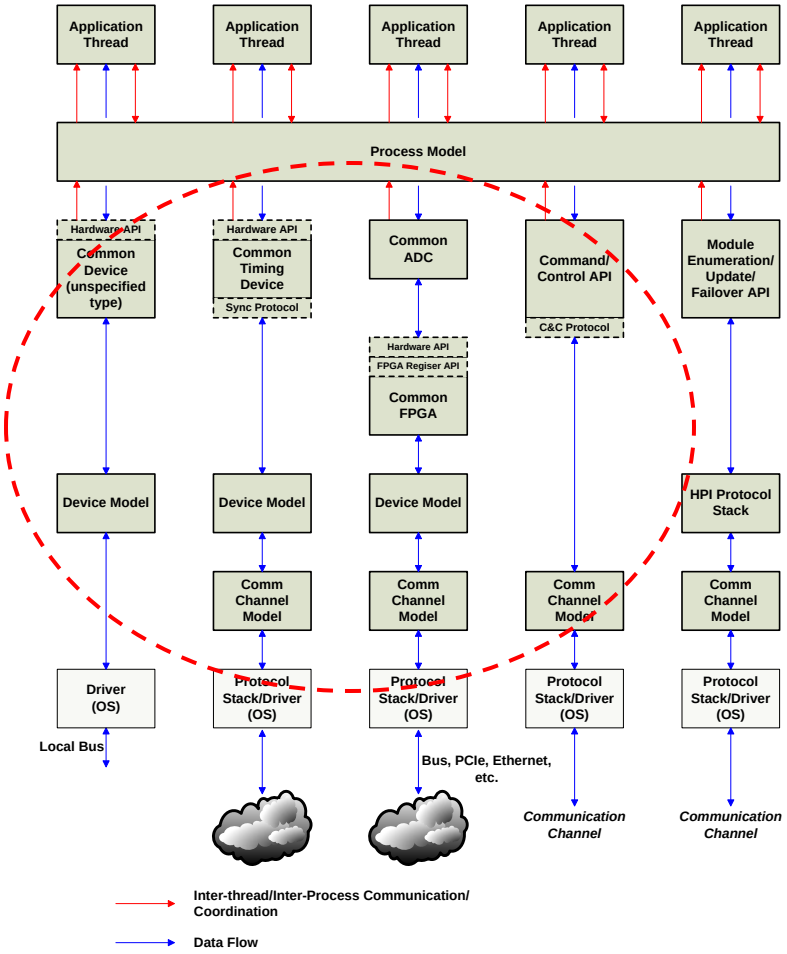


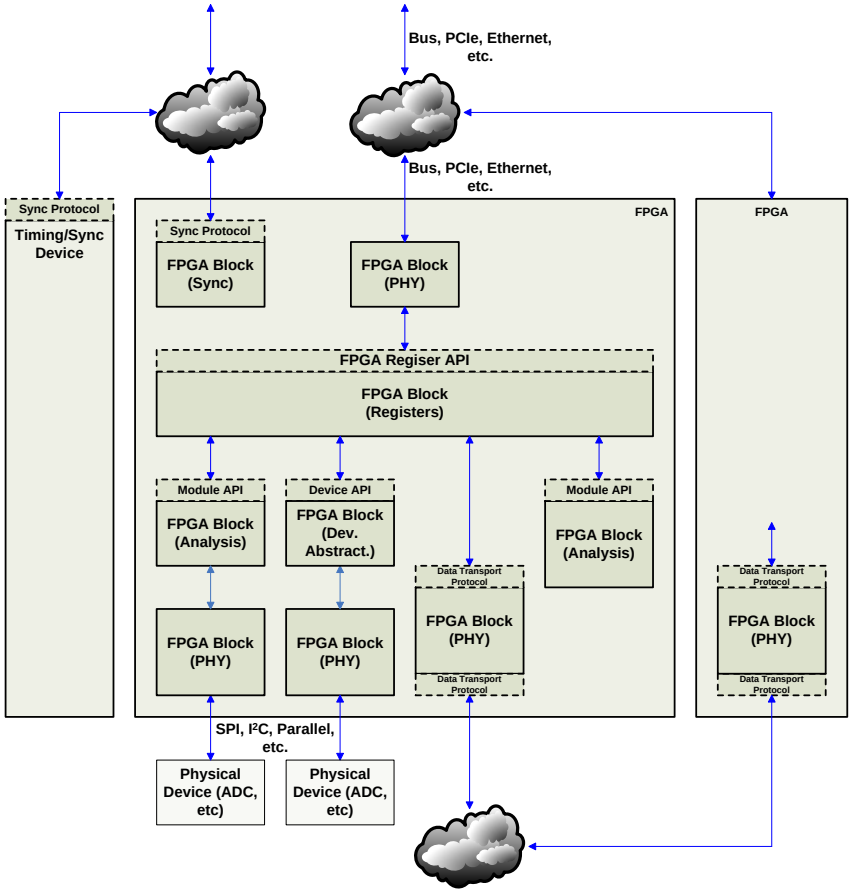
Standard Process/Thread Model



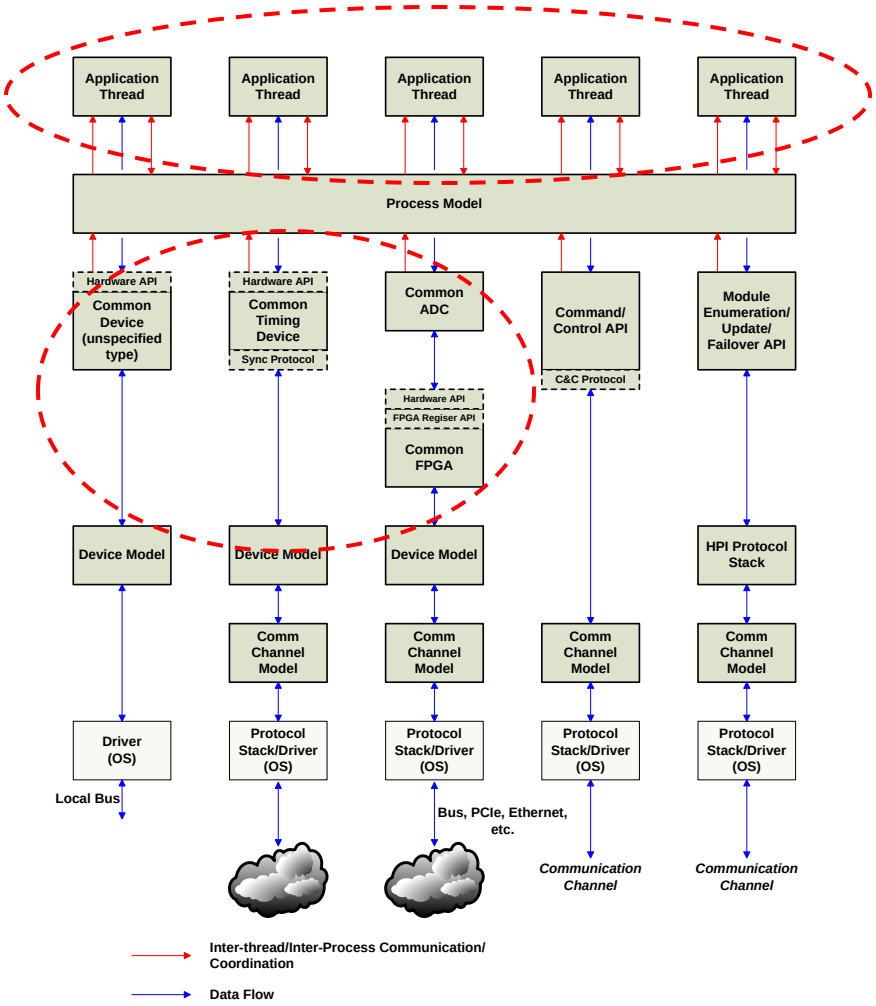


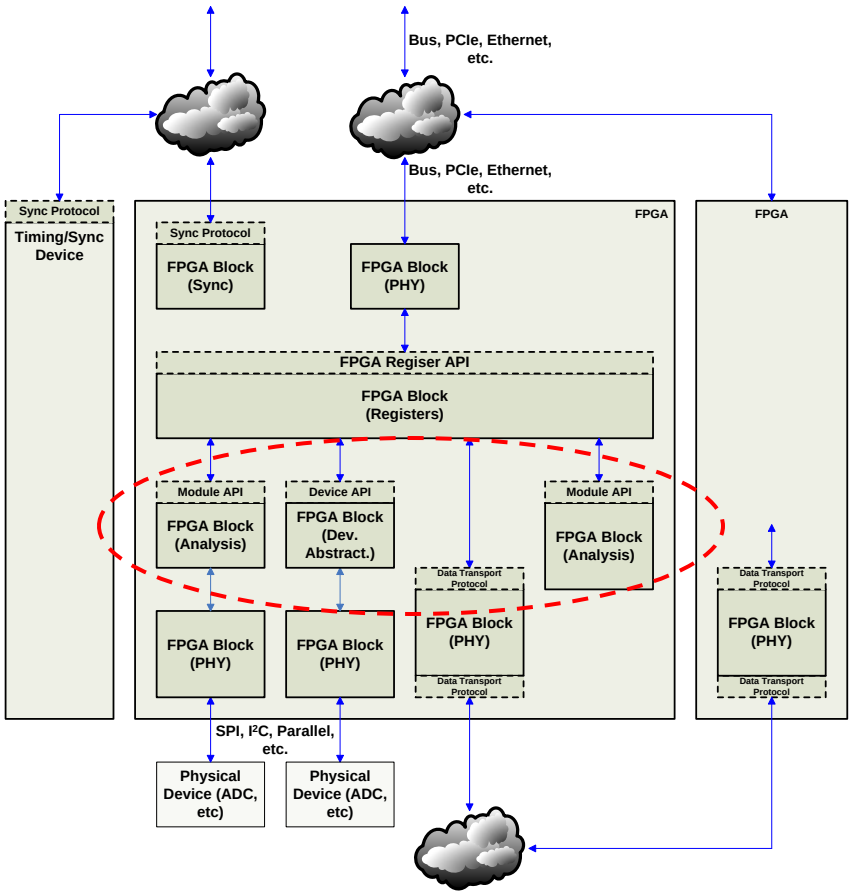
Standard Device I/O & Communications Model





Reference Designs and Templates



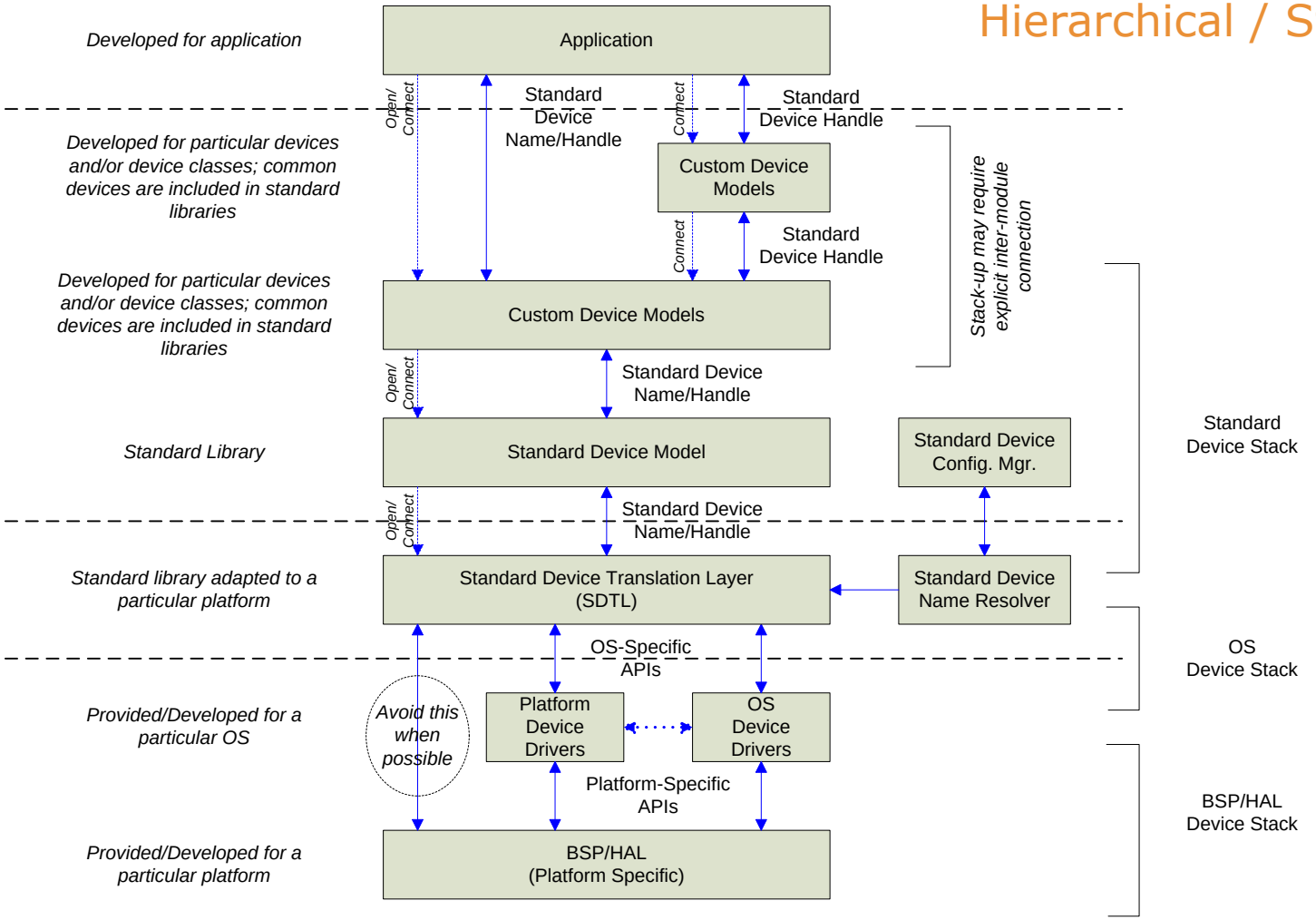


Standard Device Model – Goals

- Portability and rapid development
  - Platform-independence at the application level
    - Standard API
    - Minimal learning curve and/or platform adaptation effort
  - Device-independence at the application level
    - “Generic” device models and APIs at application I/F
      - ADC, DAC, communication channel, etc.
      - Mapped to specific devices by device object
    - Application developers may ignore many hardware details
- Hierarchical structure to facilitate complex logical device creation.
- Efficiency
  - Thin translation layer for direct access to OS/HAL devices
  - Tradeoff: Greater generality/simplicity at application API vs. higher access overhead

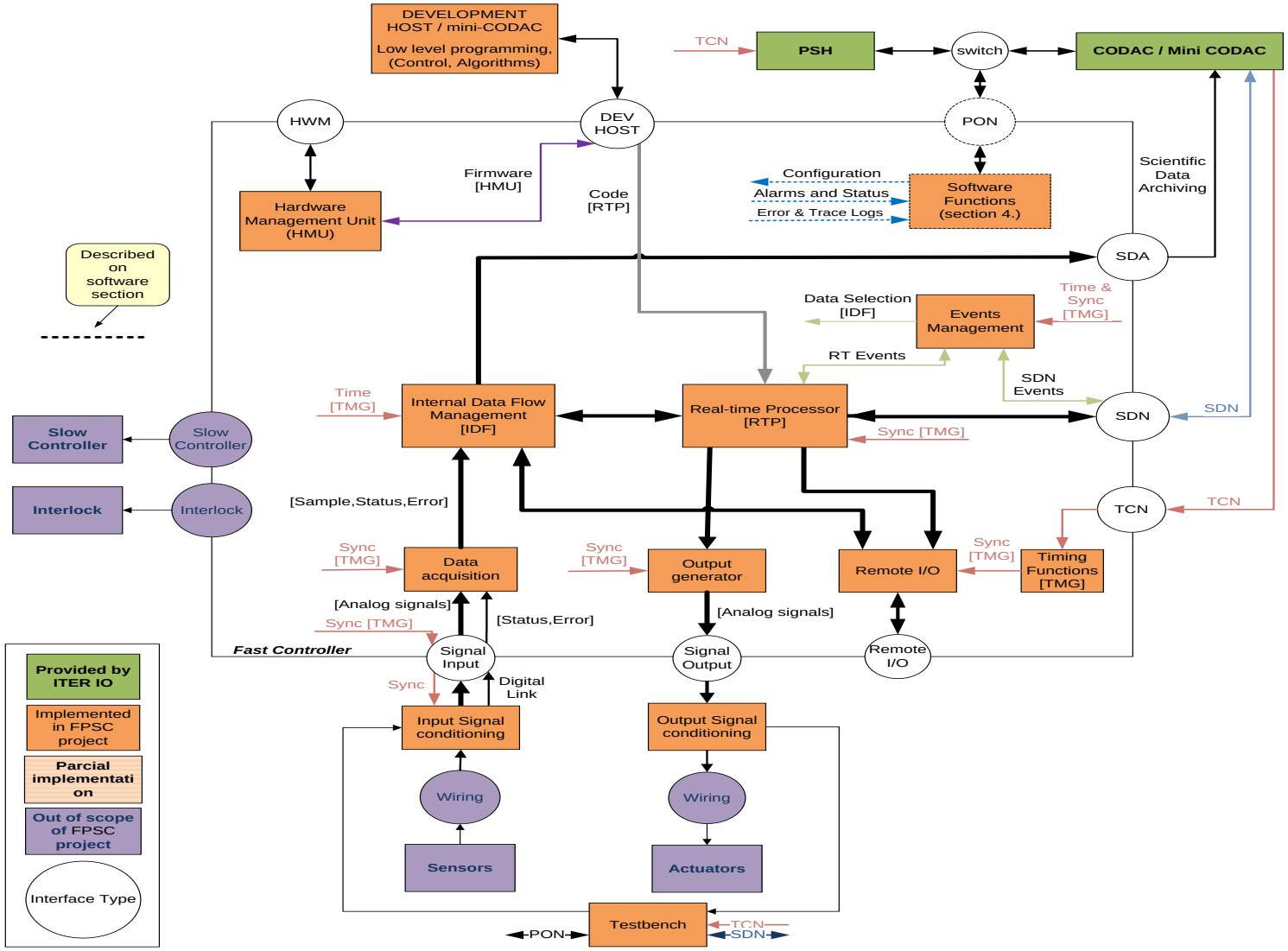
SDM Architecture

Hierarchical / Structural Model



Software Development
ITER CODAC
FPSC Prototype

Fast Plant Control System (FPSC) Functional diagram

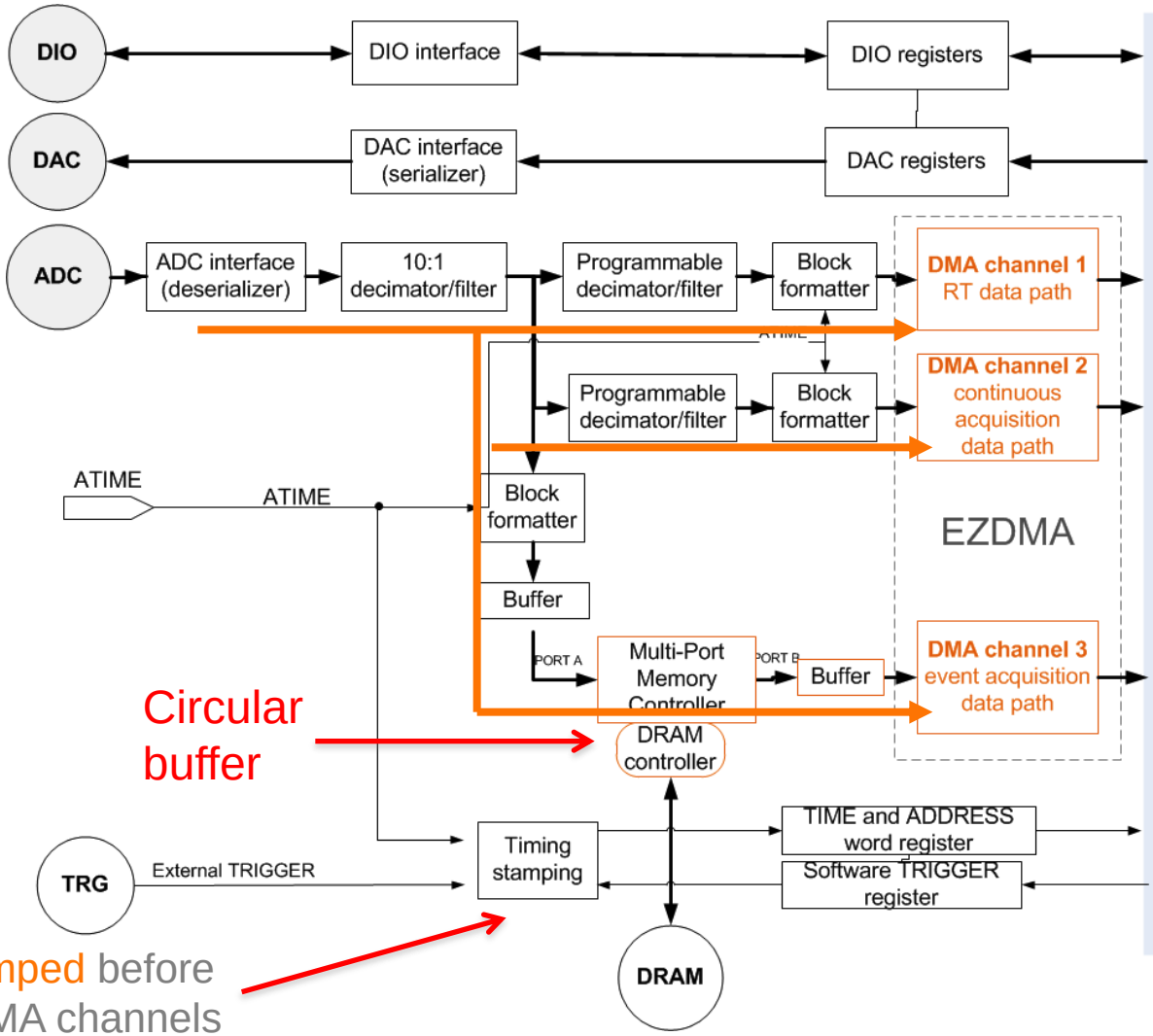


PCIe Data Routing and Data Synchronization

DMA #1
Real-time data at programmable sampling rate

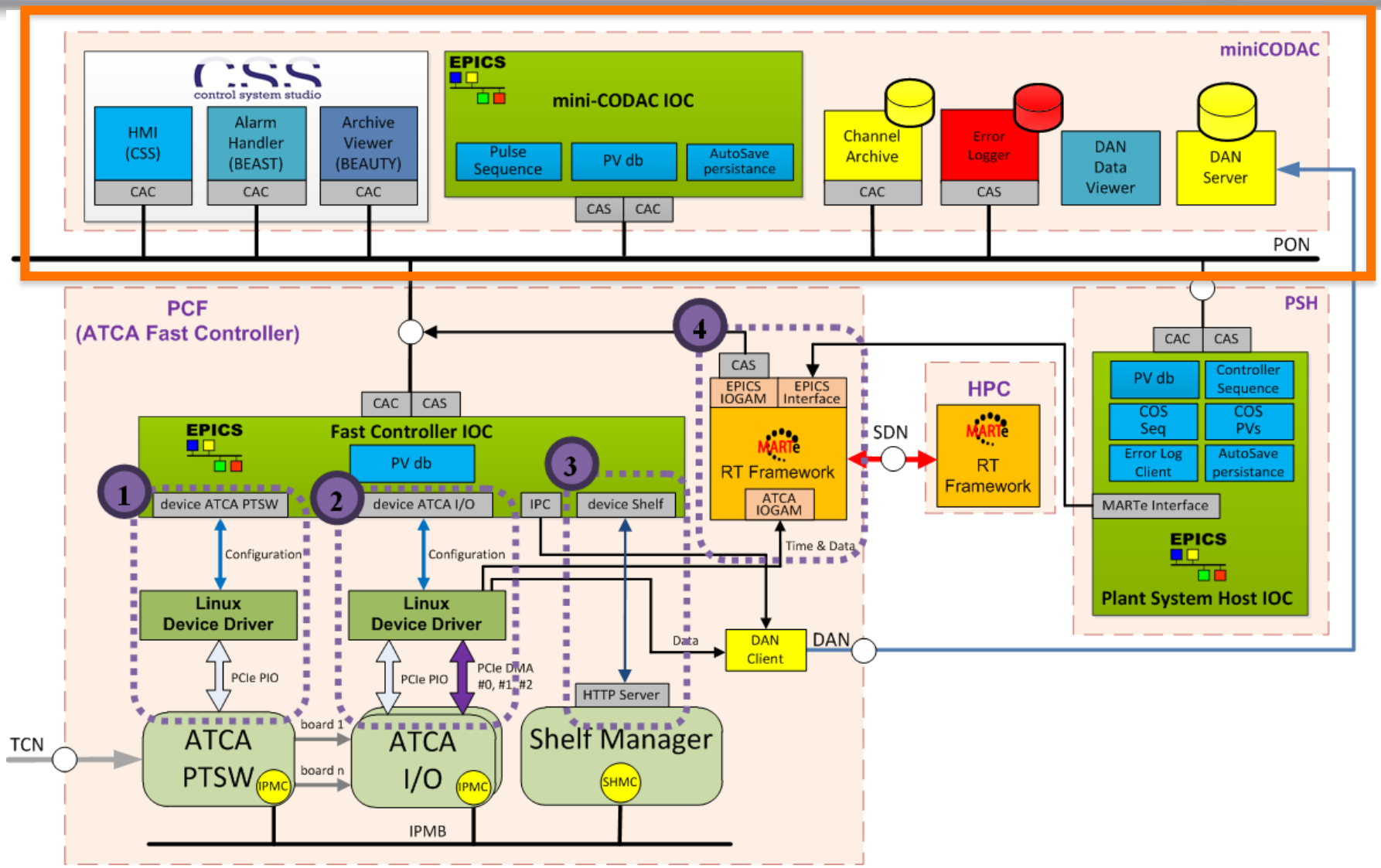
DMA #2
Data for archiving at programmable sampling frequencies

DMA #3
Data for continuous storage on the onboard memory.
Allows dynamic capture of variable rate data (around external events distributed through the RT network)

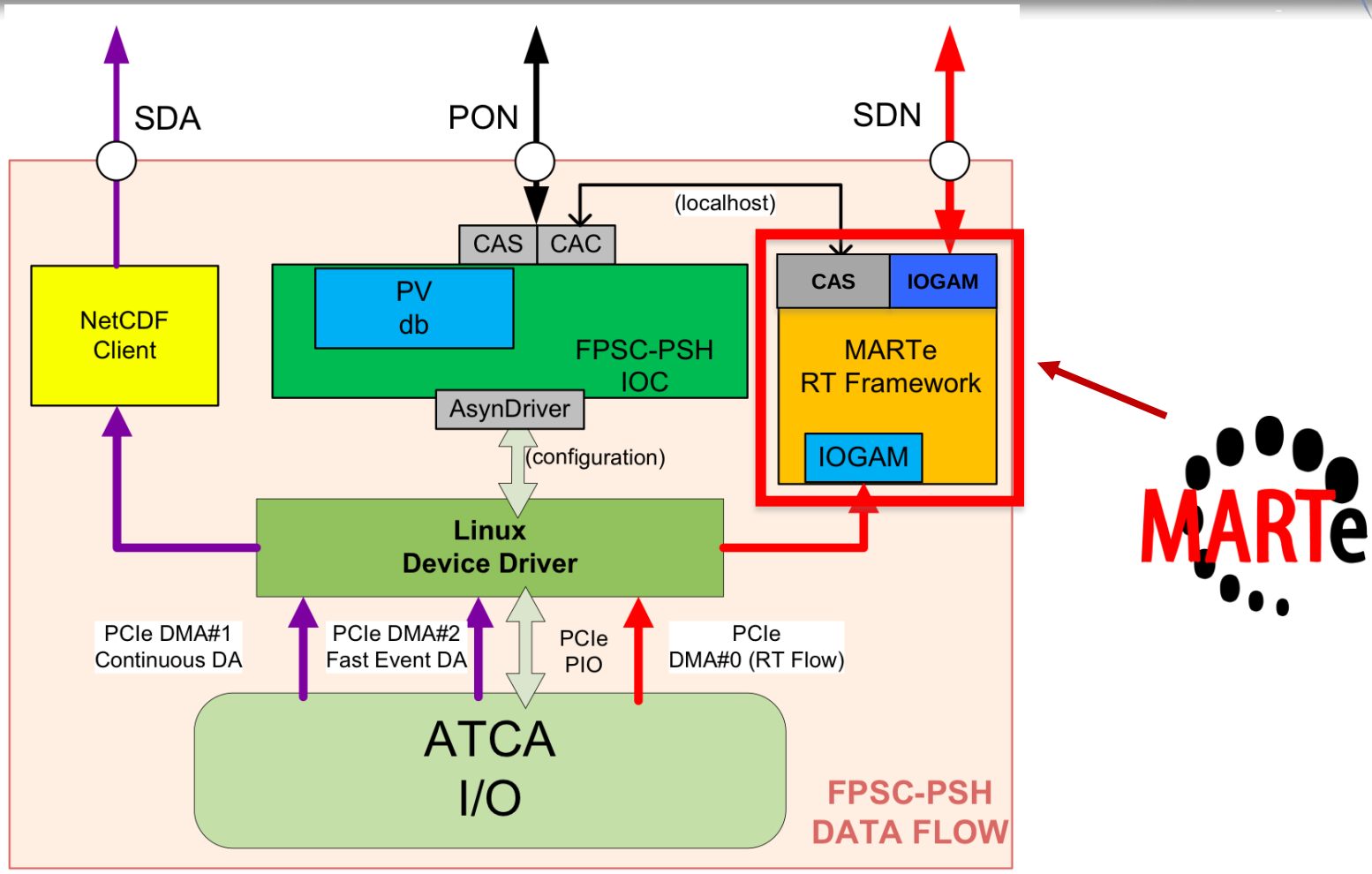


All data is time-stamped before sent through the DMA channels

FPSC Software



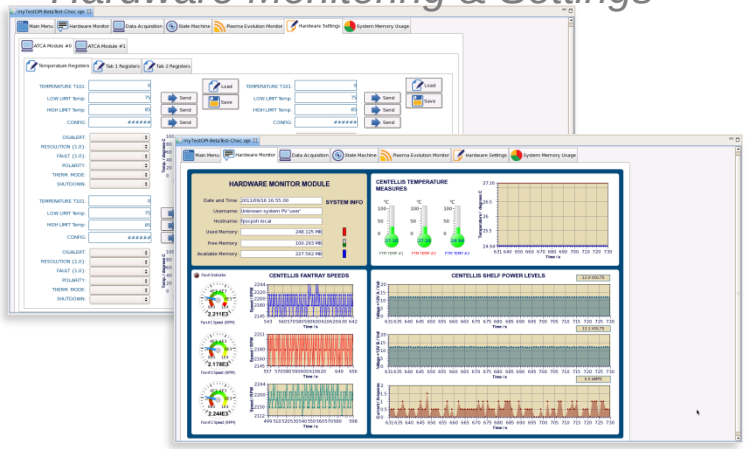
RT processing | MARTe RT framework



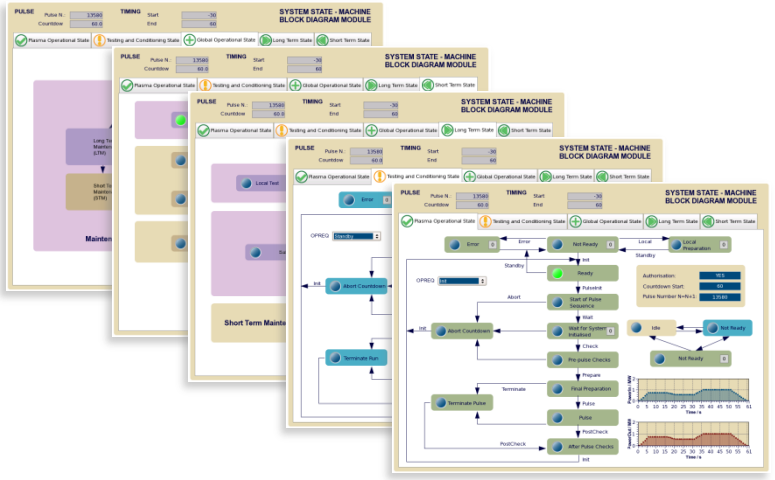
MARTe is as collection of real-time threads scheduled by an internal state machine

ITER FPSC | EPICS Human Interface

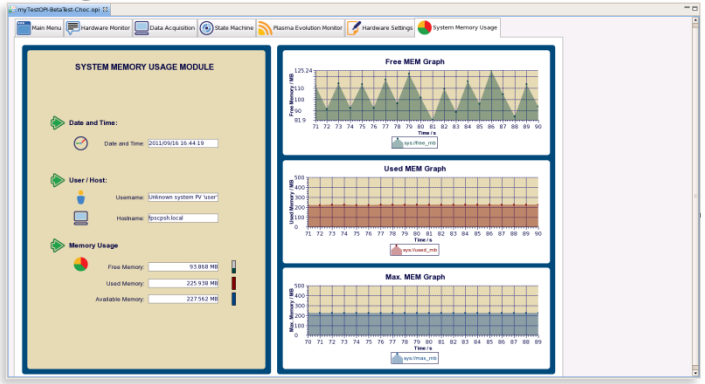
Hardware Monitoring & Settings



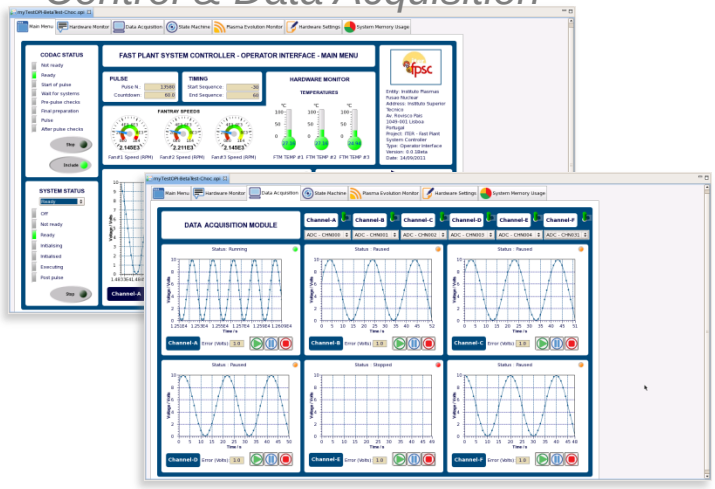
System State Machines



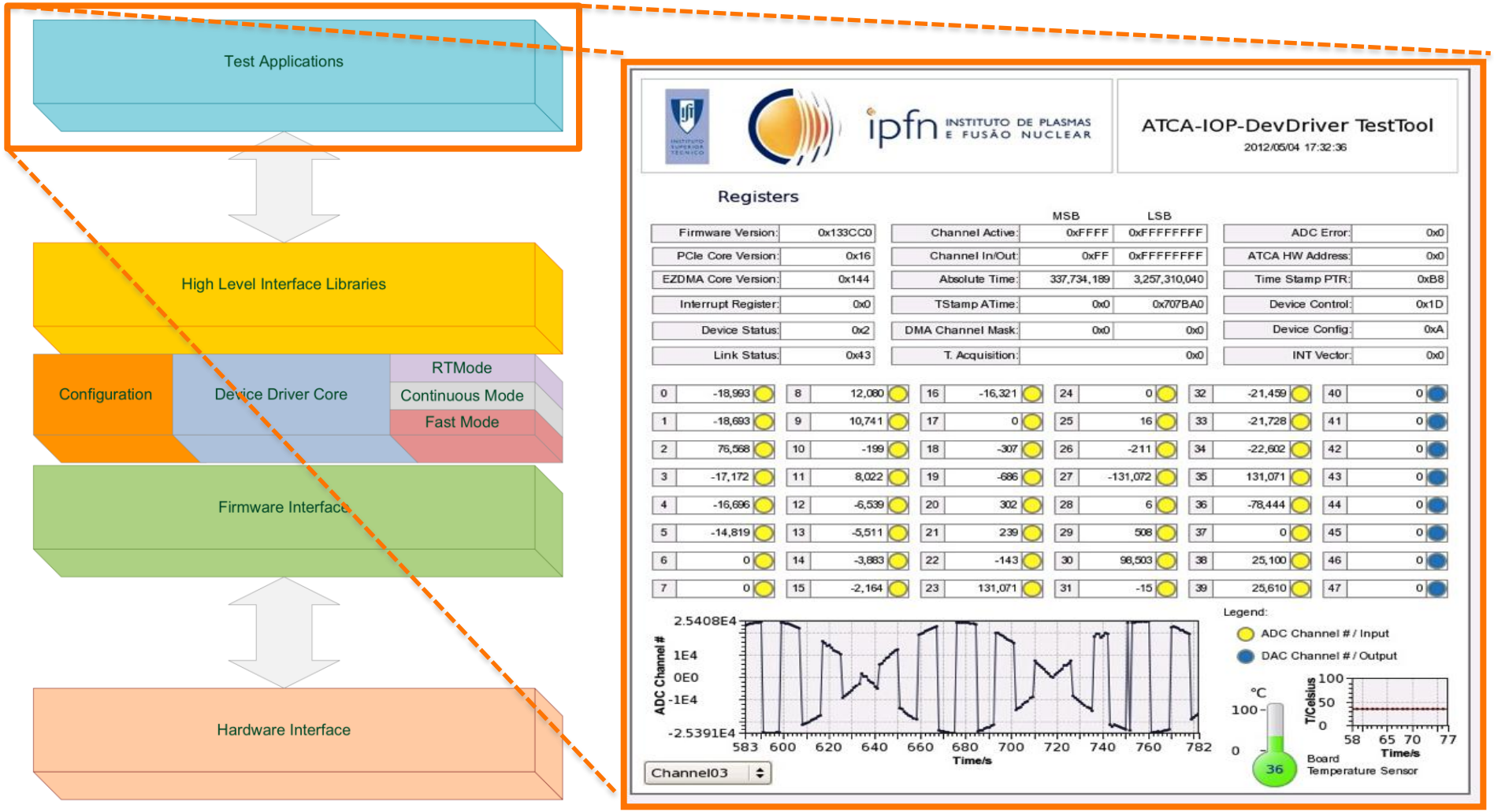
High Performance Networks Monitoring



Control & Data Acquisition



ATCA | Device Drivers & Libraries



THE END

Acknowledgments:

This work has been carried out within the framework of the Contract of Association between the European Atomic Energy Community and "Instituto Superior Técnico" (IST).

The views and opinions expressed herein do not necessarily reflect those of the European Commission.

IST also received financial support from "Fundação para a Ciência e Tecnologia" in the frame of the Contract of Associated Laboratory.

The PICMG (PCI Industrial Computer Manufacturers Group) is a consortium of companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications.

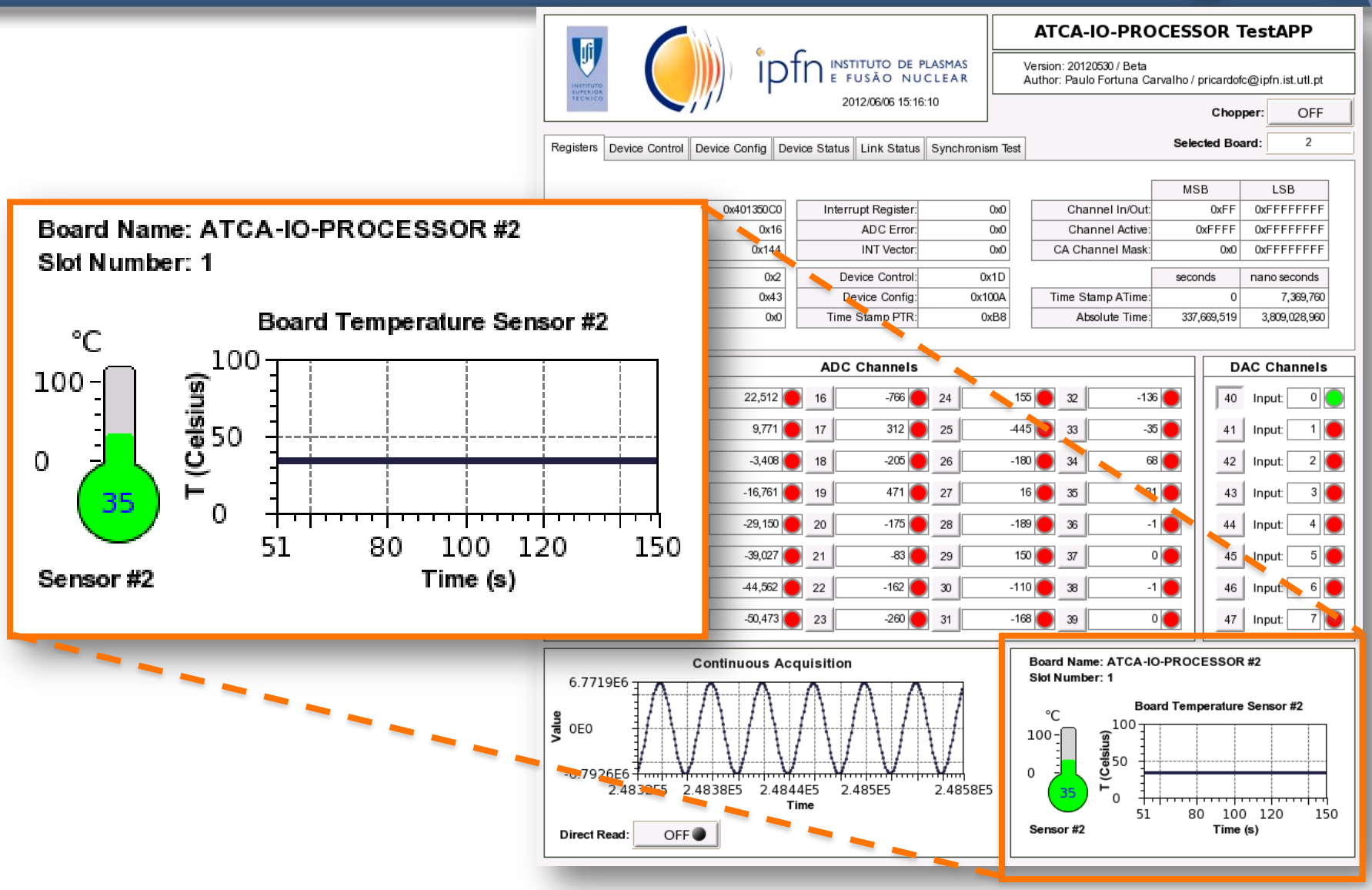
My special thanks to PICMG HWG contributors: Kay Rehlich (Desy), Ray Larsen (SLAC), J. P. Cachemiche (IN2P3) and many others.

ATCA Timing Resources

Timing over	Ports	Lines available	Performance	Compatible ATCA 3.x?
A. Bussed Clock Interface	CLK1, CLK2 assigned Only CLK3 (a,b) shall be used	6 diff pairs max	Fair 100 MHz bussed	Compatible
B. Base Interface	Ethernet hub in Slot 1 (and 2)	Timing must be encoded on Ethernet signals (IEEE1588/White Rabbit)	Good ~0.2GHz, P2P < 50 ns jitter	Changes to ATCA 3.0 may be required for WR
C. Fabric Interface	Ethernet/PCIe/SRIO hub in slots 1 (and 2)	Timing must be encoded on the data signals (Ethernet/PCIe/SRIO)	Good ~3 GHz, P2P <100 ps jitter	Compatible PCIe/SRIO timing unknown
D. Shared Fabric Interface	Hub in slot 1, (redundant Slot 2) Timing and Data lines share the same fabric port.	All nodes receive/send up to 6 (or 3 redundant) distinct timing signals.	Good* ~3 GHz, P2P <100 ps jitter	Changes to ATCA 3.x required.
E. Fabric Interface (Clock Hub)	Timing hub in slot 3(4) Ports 3(4) on node cards	All nodes receive/send up to 8 distinct timing signals	Good * ~3 GHz, P2P <100 ps jitter	Compatible
F. Update channel interface	Ports of the update channels redefined for timing	Up to 10 additional, equal length, low crosstalk diff pairs	Excellent # Low skew Low jitter	Not compatible
G. Midplane clock interface	Full-mesh of clock ports on J33 of Zone 3 (RTM).	Any board pair linked by 1 clock port (3 differential lines).	Excellent # Low skew Low jitter	Compatible

* Can be further improved on backplanes re-designed for low crosstalk noise and equal length lines.
# On backplanes designed for low crosstalk noise and equal length lines.

Remote Crate Health



Standard Hardware API – ADC topology example